13 Gb/s Si-Bipolar AGC Amplifier IC with High Gain and Wide Dynamic Range for Optical-Fiber Receivers

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Abstract—A complete linear automatic-gain-control (AGC) amplifier for a 10 Gb/s optical-fiber link was integrated on a single chip, using a Si-bipolar production technology with \( f_T \approx 22 \) GHz. It is characterized by a high gain of 37 dB, linear operation over a wide input dynamic range of 47 dB, a maximum data rate of 13 Gb/s, and a gain-independent 3-dB cut-off frequency of 10 GHz. The circuit consumes 850 mW at a single supply voltage of \(-6.5\) V. It can be operated in both a single-ended and differential mode. A novel 50-\Omega input matching circuit with only small return loss is used. Two separate output buffers with a constant output voltage swing of 500 mV allow splitting up the output signal without use of external components.

I. INTRODUCTION

A BASIC component of receivers in optical-fiber links is the main amplifier. It has to amplify the output signal of the low-noise preamplifier to an amplitude which is high enough to drive both the succeeding decision circuit and the clock-extraction circuit. Apart from high operating speed and high gain, an important demand on this amplifier is to keep the output signal amplitude constant, despite the large dynamic range of the input amplitude. If avalanche photodiodes (instead of pin diodes) are used as optical detectors or if optical-fiber amplifiers are applied in front of the photodiode, automatic-gain-control (AGC) amplifiers are usually preferred to limiting amplifiers. This is because in these cases the threshold of the decision circuit must be adjustable in order to obtain the maximum sensitivity of the receiver. (For comparison of limiting and AGC amplifiers see, e.g., [1], [2].)

The next generation of long-haul optical-fiber transmission links, just under development, will operate at data rates around 10 Gb/s. There are several papers which demonstrate that almost all monolithic integrated circuits required for such links can be fabricated in today’s Si-bipolar production technologies (e.g., [3]–[8]). However, to the best of the authors’ knowledge there is one exception: 10 Gb/s silicon AGC main amplifiers with high gain and wide dynamic range have not yet been reported.

Therefore, in this paper a single-chip dc-coupled main amplifier is described which was developed within a European R&D project [9]. This IC, which was fabricated in an advanced version of Motorola’s Si-bipolar production technology MO-SAIC V \( (f_T \approx 22 \) GHz) [10], will mainly be applied in a 10 Gb/s optical-fiber link, but it is also useful for several other applications.

The measured data, which all met the target specifications for both single-ended and differential input signals, are summarized on the top of the following page (cf. Section VII).

As mentioned before, 10 Gb/s AGC amplifiers with similar features have not yet been reported for silicon. Up to now, there is only a single Si-bipolar 10 Gb/s main amplifier but without automatic gain-control on the chip [11]. Moreover, gain \( (S_{21} \approx 12 \) dB) and dynamic range \( (\approx 16 \) dB) are much lower compared to the amplifier presented here and the peaking of the gain at the upper frequency limit is rather high (up to 7 dB). A 10 Gb/s AlGaAs/GaAs HBT amplifier with much better features has been reported in [12]. But even in this case, gain and dynamic range are smaller compared with the presented amplifier, and only part of the automatic gain control is implemented on the chip. This also holds for a 10 Gb/s GaAs MESFET amplifier module, reported in [13], which, however, needs four chips to obtain these features.

II. BLOCK DIAGRAM OF THE COMPLETE AGC AMPLIFIER

Fig. 1 shows the simplified block diagram of the complete AGC amplifier which is similar to that formerly used by our group for a 3 Gb/s circuit [14]. Because of dc coupling, differential operation is used. In the signal path there is a high-impedance input buffer stage (IB), three amplifier cells \( (A_1–A_3) \), and two decoupled 50-\Omega output buffers (OB) for driving the decision and clock-extraction circuit separately. The gain of the first two amplifier cells \( (A_1, A_2) \) is controllable while the third cell \( (A_3) \) has a constant gain. The peak detector (PD) with its external capacitor \( C_{PD} \) generates a dc voltage which depends on the output amplitude and which is compared with the output voltage of a reference network (REF), adjustable via the potentiometer \( P \) [14]. The voltage difference, \( V_{GC} \), is amplified by the gain-control circuit (GC). Its two output voltages control the gain of the first two amplifier cells. The bandwidth of this circuit is reduced by the external capacitor \( C_{GC} \) in order to avoid positive feedback. Two other external capacitors \( (C_{GC}) \) are required for the offset-control circuit (OC). This circuit is combined with a special input termination circuit (IT) that guarantees good on-chip
Maximum data rate: 13 Gb/s
3-dB cut-off frequency: 10 GHz
Maximum gain ($S_{21}$): 37 dB
Input dynamic range: 47 dB
(input voltage range from 1.4 to 330 mV${}_{p-p}$)
Equivalent input noise-voltage density (averaged up to 10 GHz): 2.5 nV/√Hz
Input return loss up to 10 GHz ($S_{11}$): $\leq -15$ dB
Two differential outputs with constant voltage swing of
(for both outputs connected in parallel)
Single supply voltage: 500 mV${}_{p-p}$
Power consumption (on chip): 800 mV${}_{p-p}$

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The two gain-controlled amplifier cells, $A_1$ and $A_2$, are shown in Fig. 2(a) and (b), respectively. For simplification, the two emitter follower pairs at each output are not shown.

The first amplifier cell ($A_1$), which is driven by an emitter follower pair (IB, cf. Fig. 1), is a four-quadrant multiplier ("Gilbert cell") extended by the stacked TIS. The lower circuit level of the multiplier in Fig. 2(a) is a TAS, while the upper level controls the gain in dependence on the dc voltage $V_{C1}$ at its input. The small-signal low-frequency voltage gain of this cell is given by [16]:

$$G_1 = \frac{\nu Q_1}{\nu I_1} = G_{01} \tanh \frac{V_{C1}}{2\gamma V_T},$$  \hspace{1cm} (1)

with the maximum voltage gain being

$$G_{01} = \frac{R_{E1}}{R_{E1} + r_e + r_b/\beta_0 + 2V_T/I_{01}}.$$  \hspace{1cm} (2)

Here, $r_e$ and $r_b$ are the emitter and base resistances, respectively, $\beta_0$ is the low-frequency current gain, $V_T$ is the thermal voltage ($= kT/q$), and $I_{01}$ stands for the source current in Fig. 2(a). The parameter $\gamma (>1)$ in (1) represents roughly the averaged influence of the emitter and base resistances on the $I_e - V_{BE}$ characteristic of the four gain-control transistors in Fig. 2(a).

Due to the high maximum input voltage swing demanded ($\Delta V_{I_{max}} = 330$ mV${}_{p-p}$) the voltage drop across $R_{E1}$ (and thus $I_{01}R_{E1}$) has to be chosen comparatively high in order to guarantee linear operation. An upper limit of the transistor currents in $A_1$, and thus of the source current $I_{01}$, is given by the degradation of the frequency response of the amplifier. On the other hand, $R_{E1}$ is one of the dominating noise sources and has, therefore, to be chosen as low as possible. As a consequence, a comparatively low value of $I_{01}R_{E1}$ was chosen which, however, at high input amplitudes results in a correspondingly high contribution of $A_1$ to the linearity error of the amplifier. This contribution can partly be compensated by use of a different circuit configuration for the second amplifier cell, as shown below.

This is because with increasing $I_{01}$ also the current through the TIS has to be increased. As a consequence, the transistor sizes must be increased (in order to avoid high-current effects), resulting in increased junction capacitances. Thus the cut-off frequency of the amplifier cell is decreased, especially by the TIS. In addition, increasing $I_{01}$ would result in a stronger loading of the input stage IB and thus in a degradation of the input matching.

III. AMPLIFIER CELLS AND OUTPUT BUFFERS

In principle, each of the three amplifier cells consists of a series connection of a transadmittance stage (TAS) with a transimpedance stage (TIS), and two to three emitter follower stages at the output, as discussed below. This configuration, which guarantees strong mismatching between succeeding stages and thus high bandwidth, is an extension of the 30-year-old proposal by Cherry and Hooper [15]. It has been used successfully in multi-Gb/s linear and limiting amplifiers [2], [14]. At high frequencies, negative feedback becomes less effective and thus mismatching is reduced. Fortunately, the input and output impedances of the cascaded stages then get a capacitive and inductive component, respectively, at each interface. This fact approaches a conjugate match and thus increases the bandwidth further.

The emitter followers are used for level shifting between the amplifier cells. Moreover, they are required for improving the mismatch between the TIS output and the TAS input, which at high frequencies is worse compared to the mismatch between the TAS output and the TIS input. Finally, they can be used for gain peaking at high frequencies.

Fig. 1. Block diagram of the complete AGC amplifier.

matching of the driving transmission line, for differential as well as for single-ended input signals.

\[1\] Here, the upper limit is given by the 1-dB compression point and the lower limit by the demanded signal-to-noise ratio. However, the full output amplitude is only obtained for an input voltage swing above 7 mV${}_{p-p}$.
output, \( V_o \), \( I_1 \), \( I_2 \)

\[ Vo = -6.5V \]

(b) Fig. 2. Gain-controlled amplifier cells: a) first cell (A1), b) second cell (A2). The two emitter-follower pairs at the outputs are not shown.

The other feedback resistor of A1, \( R_{F1} \), which well approximates the transimpedance of TIS 1, is designed for a maximum gain of \( G_{01} = 13 \) dB. The maximum admissible value of \( R_{F1} \) is limited by the high bandwidth required. The peaking capacitor \( C_{E1} \) is realized by transistor junction capacitances as described in [14]. Thus, the frequency response of the amplifier cell can be fine-adjusted via an external potentiometer by varying the dc voltage across the junctions.

The configuration of the second amplifier cell (A2), shown in Fig. 2(b), is similar to the first one. But now the lower level of the differential stages is used for gain control and the upper level, consisting of two TAS, for signal amplification. The small-signal low-frequency voltage gain of this cell is

\[ G_2 = \frac{V_{Q2}}{I_{Q2}} = G_{2a} - G_{2b} = R_{F2} \left( \frac{1}{r_{2a} + 2V_T/I_{2a}} - \frac{1}{r_{2b} + 2V_T/I_{2b}} \right) \]  

with:

\[ r_{2a} = R_{E2a} + r_e + r_b/\beta_0, \quad r_{2b} = R_{E2b} + r_e + r_b/\beta_0. \]  

Here, \( I_{2a} \) and \( I_{2b} \) are dc currents flowing into TAS 2a and TAS 2b, respectively, which depend on the control voltage \( V_{C2} \) (cf. Fig. 2(b)), and \( G_{2a}, G_{2b} \) are the transadmittances of both stages multiplied by the transimpedance \( R_{F2} \) of TIS 2. The sum of both currents equals the total (constant) source current of the second amplifier cell: \( I_{22} = I_{2a} + I_{2b} \). The maximum gain of this cell, given by:

\[ G_{02a} = \frac{R_{F2}}{r_{2a} + 2V_T/I_{2a}}, \]  

is chosen to be 8 dB.

There are two main reasons why the second gain-controlled cell uses a different configuration than the first one:

1. This technique increases the range of linear operation and thus the input dynamic range of the amplifier (without increasing the voltage drop across \( R_{E1} \)). This can be explained by using Fig. 3. In Fig. 3(a) the dc transfer characteristics (\( V_Q \) versus \( V_I \)) of the amplifier cells A1 and A2 are given (solid lines). Here the curves are calculated for a gain of A1 and A2 which corresponds to the maximum input voltage of the amplifier demanded, \( V_{Imax} = 165 \) mV (corresponding to a maximum input voltage swing of \( \Delta V_{Imax} = 2V_{Imax} = 330 \) mV). In this most critical practical case with respect to linearity errors, the maximum input voltage of A2 is \( V_{I2max} = V_{Q1max} = 92 \) mV (cf. Fig. 3(b)). The characteristic of A1 is typical of a TAS as well-known from literature (e.g., [16]). The slope of this curve decreases continuously with increasing \( V_I \) in contrast to the slope of the characteristic of A2 which increases with increasing \( V_I \) (before it approaches saturation, not shown) [17]. As a consequence, the deviations in the slope of both amplifier cells from that of a straight line partly compensate one another, resulting in an approximately constant slope over an extended range of the input amplitude. This is demonstrated by the transfer characteristic of the series connection of A1 and A2 also given in Fig. 3(a) and characterized by \( A1 * A2 \).

In Fig. 3(b) the non-linearity errors \( e_1 \) and \( e_2 \) of A1 and A2, respectively,

\[ e_\nu = \frac{\delta V_{Q\nu}}{V_{Q#\nu}}, \quad \nu = 1, 2 \]  

are given. Here, \( \delta V_{Q\nu} \) is the deviation of the transfer characteristic \( V_{Q\nu}(V_{I\nu}) \) from a straight line \( V_{Q#\nu}(V_{I\nu}) \). These straight lines are dashed in Fig. 3(a). Due to the excellent compensation (\( e_1 + e_2 \approx 0 \)), the contribution of the first two amplifier cells to the non-linearity of the total amplifier is negligible.

This unusual curve shape is obtained by subtracting the transfer characteristic of TAS 2b from that of TAS 2a (cf. Fig. 2(b)). Note that the sign of the resulting linearity error is contrary to that of a single TAS.
2. In the present design, the two gain-control transistor pairs of the multiplier cell A1 are dimensioned identically (in contrast to the design in [17]). Thus, the shape of the gain-versus-frequency characteristics and especially their 3-dB cut-off frequencies depend on the gain. An opposite dependence of the frequency response on the gain can be obtained for the second amplifier cell by an appropriate choice of the time constants $R_{E2a}C_{E2a}$ and $R_{E2b}C_{E2b}$ (here: $R_{E2a}C_{E2a}$). Thus, it is possible to compensate the gain-dependence of the frequency response of the total amplifier as confirmed by the experimental results in Section VII.

In principle, the order of A1 and A2 in the amplifier chain can be reversed. There are, however, several reasons why the first amplifier cell uses the multiplier of Fig. 2(a) and the second cell uses the modified version of Fig. 2(b):

1. Since the decoupling of the amplifier input from the input of the first amplifier cell A1 by the input emitter follower pair (IB) is limited at high frequencies, the gain-independent input impedance of the multiplier (A1) is advantageous. This especially holds with respect to a small and gain-independent input return loss.

2. The multiplier (A1) shows a better common-mode signal behavior than the modified version (A2). This feature of the first amplifier cell is advantageous when the amplifier input is driven by a single-ended signal.

3. Only two (instead of three) emitter follower stages for level shifting are required between A1 and A2.

In contrast to A1 and A2, the third amplifier cell A3 (cf. Fig. 1) has a constant gain. Again, this cell consists of a transadmittance stage with peaking capacitors and a transimpedance stage. But now three succeeding emitter follower stages are required to drive the two separate output buffers (OB) without essential loss of bandwidth. In modification of the simplified block diagram of Fig. 1, the offset-control circuit (OC) is driven by the first emitter-follower pair and the peak detector (PD) by the second emitter-follower pair.

The output buffers are transadmittance stages, again with peaking capacitors shunted to the emitter series resistors. An on-chip output termination resistor of 150 Ω is provided in order to reduce the output return loss compared to open collectors. The differential output voltage swing of each buffer is nominal 500 mVp-p. By shunting both buffers this swing is increased to 800 mVp-p (across the unchanged 50-Ω load) and the on-chip output termination resistance is reduced to 75 Ω further reducing the return loss.

IV. GENERATION OF THE GAIN CONTROL VOLTAGES

The basic principle of the automatic gain control has already been discussed in Section II using Fig. 1. The control voltages of A1 and A2 have to be adjusted in such a manner that the output voltage swing (500 mVp-p) does not depend on the input voltage swing. For this, a peak detector (PD) measures the actual peak output potential of A3 which is related to the signal amplitude. It consists of an emitter-follower pair with connected emitters which drive the external capacitor $C_{PD}$. This capacitor is charged to a voltage which equals the maximum value of both complementary inputs of the PD minus the forward base-emitter voltage. This voltage is compared with the nominal value of the peak voltage which is generated by a reference network (REF) and which is related to the nominal output amplitude of the AGC amplifier. For choosing the right value of the reference voltage, the voltage gain of the output buffers has to be taken into account. By use of an external potentiometer $P$ (see Fig. 1) the reference voltage and thus the output amplitude of the amplifier can be varied.

The voltage difference, $V_{GC}$, between the output of the reference network and of the peak detector, i.e., the deviation from the nominal value, is amplified by a differential dc amplifier (GC) with high gain ($\approx 60$ dB). It generates two different gain-control voltages ($V_{GC1}, V_{GC2}$) for the two first amplifier cells, which depend in a quite different manner on the input amplitude. This is because both the control characteristics and the overlapping of both control ranges have to be optimized with respect to maximum dynamic range for linear operation. E.g., starting from the minimum input amplitude (i.e., maximum gain) and increasing this amplitude, first the gain of A2 is much more reduced than that of A1. At high input amplitudes, where the gain of A2 has nearly reached its minimum value, the amplifier gain is mainly determined by

4 Line matching at the output by using a 50-Ω on-chip resistor is not required here. This is because in the intended application the amplifier drives a decision circuit with a well defined 50-Ω input impedance, so that the influence of the undesired double reflections is only small (cf. [41],[18]). On the other hand, 50-Ω output matching would reduce the gain of the amplifier. As a consequence, an additional gain cell would be required, resulting in reduced bandwidth and increased power consumption.
A1. This behavior, which also improves the noise behavior of the amplifier, is obtained by providing an appropriate offset-voltage source within the gain-control circuit (GC).

Special precautions were taken to make sure that the output voltages of the GC circuit do not change their polarity, since this would result in an incorrect operation. Moreover, in order to avoid positive feedback in the closed loop at higher frequencies, the bandwidth of this circuit was drastically reduced by an external capacitor ($C_{GC}$).

V. OFFSET CONTROL AND INPUT TERMINATION CIRCUIT

Automatic offset control is mandatory for high-gain decoupled amplifiers. Fig. 4 shows the main part of the offset-control circuit (OC) which is combined with the input-termination circuit (IT). The low-pass characteristic of the OC, required for suppressing the feedback of the high-frequency signal to the amplifier input, is mainly obtained by the on-chip components, $R_1$, $R_2$, and $C_1$, the bond inductors, $L_{OC}$, and the external capacitors, $C_{OC}$. At high input amplitudes the gain of both $A1$ and $A2$ is low, resulting in a low gain of the closed offset-control loop. As a consequence, the offset-control circuit presented is less effective than with low input amplitudes. Therefore, an additional offset control circuit (not shown in Figs. 1 and 4) is used which achieves dominating influence at high input amplitudes. For this, the voltage difference between the nodes $N1$ and $N2$ in Fig. 4 is amplified by an emitter coupled pair and converted into a control current, which is fed into the input nodes, $N3$ and $N4$ of TIS 2 in Fig. 2(b).

On-chip matching of the driving 50-$\Omega$ transmission line is preferred to matching by external resistors. The novel IT circuit is suited for both differential and single-ended operations. In contrast to some other approaches (e.g., [14]), it allows combining on-chip matching, biasing of the input stage IB, and effective offset control (i.e., including the input stage) without increasing the equivalent input noise. Moreover, it guarantees stable operation under arbitrary bias conditions. Its input impedance is given approximately by the series connection of $R_S$ (40 $\Omega$) and the output impedance of the emitter followers EF. The increase of the latter at high frequencies is limited by use of $C_2$. For differential operation, the bond inductance $L_B$ can be simply adjusted to the input capacitance of the amplifier (including the bond-pad capacitances $C_{pad}$) with respect to the characteristic impedance of the driving transmission line [18]. For single-ended operation the influence of the ground bond inductance $L_G$ and the input impedance of IB (which is changed compared to differential operation) must be compensated by an (adjustable) on-chip capacitance $C_I$. The input return loss at high frequencies can be reduced further by use of a small external capacitor $C_{EX}$, at a correspondingly reduced $C_I$. $C_{EX}$ can, e.g., be realized in a simple manner by broadening the end of the driving strip line.

VI. ADDITIONAL REMARKS ON CIRCUIT DESIGN

The amplifier was carefully designed on the base of preliminary data of an advanced version of Motorola's MOSAIC V process [10], considering worst-case conditions and a range of the junction temperature from 20-90°C. The main improvements compared to the standard MOSAIC V process are caused by the selectively implanted collector region (SIC) which increases both the admissible collector current density and the transit frequency of the transistors ($f_T \approx 22$ GHz). Four metallization levels are provided.

It should be pointed out that this high-gain amplifier must be operated near the speed limit given by the technology. Therefore, besides the circuit currents and resistances, the configurations and dimensions of the transistors have to be optimized individually also. In the circuit simulations, which were performed by use of SPICE 2G7, all the parasitic on-chip metallization capacitances and bond inductances were considered. Moreover, a new high-frequency transistor model was applied which takes into account non-quasi-static transistor behavior and high-frequency emitter current crowding [19].

The circuit was mainly designed with regard to optimum output eye diagrams, up to the desired data rate and for the total (wide) dynamic range. Furthermore, in order to extend the possible range of applications, gain-independent flat gain-versus-frequency responses at constant cut-off frequencies and good linearity were aimed at. Optimum eye diagrams at maximum data rate are obtained if the different (loaded) amplifier cells as well as the output buffer have about the same cut-off frequency and nearly constant gain and group delay up to the upper frequency limit.

Fig. 5 shows a photograph of the amplifier chip. To minimize crosstalk on the chip as well as feedback via ground and supply bond-inductances the following measures were taken:

1. All the cells in the signal path of the amplifier (i.e., IB, A1–A3, OB, cf. Fig. 1) are arranged in a straight line with sufficient distance between these cells on the chip (cf. Fig. 5). As a result, the output pads are far away from the input pads reducing interaction between these terminals. Moreover, due to the exact symmetry with respect to this straight line, generation and influence of common-mode noise is reduced.

2. The bias voltage generators for the transistor current sources are separately provided for the different amplifier cells in order to avoid interactions via these networks.

3. Around each cell there are two wide metallization rings in different levels, one in the 4th metallization level and the other in the 3rd metallization level. These rings are connected by wide metallization lines (again in both the 4th and 3rd metallization level) to the ground and supply-voltage pads, respectively. Thus an on-chip capacitor
Fig. 5. Photograph of the amplifier chip (1.8 mm x 1.4 mm). Most of the bond pads are provided for test reasons only and are, therefore, not required for normal operation.

\( \approx 10 \text{ pF} \) between the supply voltage and ground is obtained, with the consequence that decoupling of the supply voltage by external capacitors is no longer necessary. There is only a single contact between the rings and the corresponding ground and supply lines, respectively, which is located on the symmetry line of the chip. By this measure and an additional connection (on the symmetry line) between succeeding ground rings the influence of common-mode noise (e.g., caused by the ground bond-inductances) is considerably reduced.

Moreover, each supply-voltage ring is connected on its whole length to the underlying p+ substrate in order to reduce coupling via the substrate.

4. Around the whole chip there is a wide ground metallization ring which allows bonding at arbitrary points. Thus optimal multi-bonding is possible reducing the effective bond inductance considerably.

These measures have proven to be sufficient for avoiding any interaction and instability problems. Even low-frequency measurements of the amplifier on the wafer are possible using a wafer prober with simple needle probes.

VII. MEASURING RESULTS

For high-frequency measurements the chip was mounted on a ceramic substrate with 50-\( \Omega \) strip lines and SMA-connectors using a conventional bonding technique. For the capacitances shown in Fig. 1, cheap surface mount (SMD) capacitors are sufficient. According to the simulation, no bypass capacitors for decoupling the supply voltage are required. This advantage is the result of the measures described in Section VI.

It should be noted that the experimental results presented in the following were all achieved by the first technological run and without any redesign. This fact and the good agreement between simulated and measured results confirm the reliability of the simulation predictions.

Fig. 6 shows the dc transfer characteristics, i.e., the output voltage \( V_Q \) versus the input voltage \( V_I \), with the amplifier gain \( G \) as a parameter (\( G \) being the low-frequency value of \( S_{21} \)). Since (besides the automatic gain control) the offset control had to be switched off for this measurement, a small offset voltage is normally observed which, however, is compensated here by an external voltage. A good linearity of the characteristics over a wide range of \( V_I \) can be observed, as a result of the design concept discussed in Section III. Here, the maximum input voltage swing over which \( V_I \) can be observed, is defined by the 1-dB compression point of the output voltage.\(^5\)

Fig. 7 shows the gain-versus-frequency characteristics within the total dynamic range of interest. This figure demonstrates the wide gain-control range of the amplifier (here: 60 dB). Note, that for all characteristics the gain is rather flat and the cut-off frequencies are nearly equal (about 10 GHz) as expected from the design proposals discussed in Section III.

Of course, for this measurement the automatic gain-control had to be switched off again, so that the relationship between the gain and the input amplitude is lost. Instead, the voltage \( V_G \) (see Fig. 1) and thus the gain is now adjusted via an external voltage source.

Even more important for the intended application are the output eye diagrams at the nominal data rate of 10 Gb/s, which are shown in Fig. 8 for two considerably different input amplitudes. For this experiment the amplifier was driven by a pseudo-random pulse-generator with a sequence length of \( 2^{15} - 1 \) bits [20]. Well-opened "eyes" and small time jitter can be observed. Even at 13 Gb/s acceptable eye diagrams are obtained as demonstrated in Fig. 9. To the best of the authors’ knowledge, this is the highest data rate reported up to date for a linear AGC amplifier in any IC technology.

It should be mentioned that it makes nearly no difference in the dc and high-frequency measuring results whether the input is driven by single-ended or differential signals.

Fig. 10 shows the input return loss (\(|S_{11}|\)) of the amplifier for both single-ended and differential input signals. It is lower than -15 dB for both operation modes up to 10 GHz. As

\[ \Delta V_I \leq \Delta V_{I_{\text{max}}} \] linear operation is guaranteed even if the adjusted gain is so low that the output amplitude no longer reaches its nominal value \( \Delta V_Q = 500 \text{ mV}_{p-p} \).
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Fig. 7. Gain-versus-frequency characteristics (|S_{21}|). The 3-dB cut-off frequencies are marked by circles. For this measurement the automatic gain-control is switched off.

Fig. 8. Output eye diagrams at 10 Gb/s for input voltage swings $\Delta V_I = 10 \text{ mV}_{p-p}$ (top) and 300 mV$_{p-p}$ (bottom). Time scale: 40 ps/div. The output amplitude in both cases is 500 mV$_{p-p}$.

Fig. 9. Output eye diagrams at 13 Gb/s for input voltage swings $\Delta V_I = 10 \text{ mV}_{p-p}$ (top) and 300 mV$_{p-p}$ (bottom). Time scale: 30 ps/div. The output amplitude in both cases is 500 mV$_{p-p}$.

Fig. 10. Input return loss (|S_{11}|) for single-ended (solid line) and differential operation (dashed line).

mentioned before, for the intended application the output return loss is of minor importance. For differential operation the measured $|S_{22}|$ is below $-6 \text{ dB}$ up to 16 GHz. For single-ended operation $|S_{22}|$ is below $-6 \text{ dB}$ up to 3 GHz and below $-12 \text{ dB}$ from 3 to 16 GHz.

Finally, the noise performance of the amplifier was measured. From dc to 8 GHz the equivalent noise voltage density related to the input, $v_{N,I}$, varies between 2 and 2.6 nV$/\sqrt{\text{Hz}}$ only, before it strongly increases to higher frequencies (e.g., 4 nV$/\sqrt{\text{Hz}}$ at 10 GHz). For this amplifier the noise bandwidth can be approximated by the 3-dB cut-off frequency. Then the resulting averaged noise voltage density is $v_{N,I} \approx 2.5 \text{ nV$/\sqrt{\text{Hz}}$}$. This value is slightly lower than the simulated value since in SPICE the correlations between the different noise sources are not considered. It is sufficiently low not to degrade the sensitivity of the complete receiver in the optical-fiber link, which is thus determined by the front end only [21].

VIII. SUMMARY

A dc-coupled linear AGC amplifier with a record data rate of 13 Gb/s and a bandwidth of 10 GHz has been realized in a Si-bipolar production technology. In contrast to other gain-controllable amplifiers developed for receivers in 10 Gb/s optical-fiber links, the complete amplifier is integrated on a single chip. Moreover, it stands out for high input dynamic range, high gain, flat gain-versus-frequency response, low input return loss, and two separate output buffers.

The basic circuit configuration used for the wide-band gain-controllable amplifier cells is that of a four-quadrant multiplier extended by a transimpedance stage and two emitter follower pairs. By use of a modification of the multiplier configuration for the second amplifier cell, the range of linear operation is extended and the usually strong dependence of the cut-off frequency on the gain can be compensated. A low input
return loss for both single-ended and differential input signals is obtained by a novel on-chip determination circuit which is combined with the offset-control circuit.

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