A NEW HIGH EFFICIENCY CMOS VOLTAGE DOUBLER

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ABSTRACT
A charge pump cell is used to make a voltage doubler using improved serial switches. The PMOS transistor used for the serial switch is analyzed and a model suitable for simulation is described. The importance of capacitors is shown with plots of efficiency versus load and stray capacitors. Several problems arising at low voltage or high frequency are developed and some optimizations are presented. The substrate current is totally suppressed by the technique of bulk commutation. An efficiency of 94% has been reached using external capacitors.

1. INTRODUCTION
The need for voltage elevators has increased with the apparition of circuits operating from single battery cell. But their principle does not allow a high level of efficiency in standard CMOS technologies. A circuit that can work in a CMOS technology as a clock booster has been already proposed [1]. This circuit has the particularity of connecting n-transistors from their source (Fig. 1). This use of NMOS is efficient, not only because of carrier speed, but particularly for automatic reverse bias of the junctions. Unfortunately, with this circuit, to make a fixed doubled output we need a serial switch and this can only be achieved by a PMOS transistor because of the $V_T$ drop. The problem arising with the use of PMOS is to ensure the reverse bias of the junctions.

Fig. 1: Charge pump cell from [1]

A solution was proposed in [2] showing a method using two step-up blocks, one for the supply and the second only to boost the bulk voltage of P1 (Fig. 2). This solution totally prevents a direct biasing of PI junctions but does not solve the problem for P2. In the second step-up, the P2 bulk is just connected to a capacitor, and thus is floating. Therefore, P2 bulk voltage will rise with junction currents. This implies that the drain to bulk voltage of P2 stays close to the junction potential. The result is a quasi permanent charge loss. Of course, this loss is not very important compared to the whole efficiency of the step-up. Nevertheless, a much better solution, providing no loss whatsoever in the junctions, is presented. This solution requires only two minimal transistor and no second step-up.

Fig. 2: Fixed output charge pump with PMOS bias [2]

In addition, we suggest several optimizations to improve efficiency. Some are very important at low voltage, others at high frequencies. The maximum efficiency reachable is calculated and plotted for all types of integrated capacitors.

In the study presented here, we analyze the problem of serial switches for an Nwell process only. For a Pwell process, everything is inverted, and only negative voltages can be generated.

2. MODELLING
The cross-section of the PMOS in a p-substrate is shown in Fig. 3 with its equivalent schematic. We represent three parasitics elements which are: two vertical bipolars and a lateral bipolar.

12.2.1
The vertical bipolars always account for parasitics while the lateral bipolar, when the PMOS is ON, can be seen as an improvement in conductance. Of course, when the PMOS is OFF, it is also a parasitic device. It is unclear whether we should favour the lateral over the vertical bipolar or not. To answer this question, we need to establish a model of the PMOS with its parasitics. Fig. 4 recalls the standard SPICE DC models for a MOS transistor. It is not suited to our purpose because the well is not taken into account.

To produce an appropriate model, it is necessary to add the SPICE controlled current sources corresponding to the bipolars. To make an understandable and clear schematic, the base resistors are neglected (Fig. 5).

A DC model can be implemented using simple MOS and bipolar equations for the current sources but it is simpler to suppress the junction diode in a standard MOS model and to add the bipolars in the schematic. This can be done simply by setting the saturation current to zero in the parameter list for the PMOS. The most difficult task is to find the correct values for IS and β of the bipolars. These parameters are hard to find because of their dependence on the technology and their large variations due to poor control over well doping. Accordingly, some typical values can be used to simulate the effect of the parasitic bipolars, but neither good absolute values nor good ratios between lateral and vertical bipolars can be obtained. The junction capacitances can be modelled either by the MOS model or by the bipolar model. In any case, this paper present a solution to eliminate these parasitic effects, and so an accurate modelisation is not necessary.

3. PRINCIPLE
To eliminate the effect of the vertical bipolars, the only possible solution is to tie the well at the highest voltage between source and drain. The schematic diagram used for fulfilling this function is shown in Fig. 6.

To keep parasitic elements to a minimum, M1, M2 and M3 must share the same bulk. Of course, the problem is only solved with proper control of M2 and M3, which must select the highest voltage between source and drain. There is not a unique solution for solving this problem and it depends upon the application. In the next paragraph we show the use of this technique for the charge pump cell presented in [1].

4. REALIZATION
The voltage doubler described in the introduction can be dramatically improved by using a dual serial switch and the principle of bulk commutation (Fig. 7).
absolute necessity, because VoUT must always stay between 2VIN and 2VIN - Uj, to avoid the turn-on of the vertical bipolar. With M5 and M6, COUT is only present to smooth the output voltage, and so is not indispensable. The C B capacitor is small but necessary to preserve the bulk potential when switching.

The source resistance is given by: 
\[ R_s = \frac{1}{2 \cdot f \cdot C} \]  
(1) [4]

without taking COUT into account. The factor 2 comes from the two capacitors C1 and C2, which act at each phase of the clock. It is also assumed that the voltage drop of M1 through M4 is negligible.

Efficiency is given by: 
\[ \eta = \frac{E_L}{E_L + E_S} \]  
(2)

\[ E_L : \text{energy given to load} \]
\[ E_S : \text{energy loss} \]

with: 
\[ E_L = \frac{V_{OUT}^2}{f \cdot R_L} \]  
(3) 
\[ E_S = 2 \cdot C_S \cdot V_{IN}^2 + 2 \cdot C \cdot \Delta V_{OUT}^2 \]  
(4)

\[ \Delta V_{OUT}: \text{VoUT drop due to } R_S \]

and: 
\[ V_{OUT} = 2 \cdot V_{IN} \cdot \frac{R_L}{R_L + R_S} \]  
(5) 
\[ C_S = \alpha \cdot C \]  
(6)

C_S : bottom plate stray capacitor of C, R_L : load resistor

Resulting in: 
\[ \eta = \frac{1}{1 + \alpha \cdot C \cdot f \cdot \frac{(R_L + R_S)^2}{2 \cdot R_L} + 2 \cdot C \cdot f \cdot \frac{R_S^2}{R_L}} \]  
(7)

The maximum is reached for: 
\[ R_L = R_S \cdot \sqrt{\frac{1}{\eta} + \frac{\alpha}{4}} \]  
(8)

5. OPTIMIZATIONS

To improve efficiency, several points must be studied. The most important part of this step-up, from an efficiency point of view, are the capacitors. If integrated, they always have a stray capacitor to the ground, even if we use a silicon on insulator technology (SOI).

**Integrated capacitors**

When running at voltages below the maximum voltage recommended by the process, the best thing to do is to use thin oxide capacitors. They provide about 15% stray capacitance and have a high capacitance per area. A second very efficient solution is the use of double poly technologies, although they have a lower capacitance per area than thin oxide, they have the smallest stray capacitance at about 5%. It seems that this value is close to the value of thin oxide capacitors realized in SOI technology. At low voltage, below 1.5V, the dip of the MOS capacitance can be bothersome. In this case, we recommend the use of double poly capacitors. Efficiencies are plotted versus load and \( \alpha \) in Fig. 8 and Fig. 9.

For the ideal case, modeled by \( \alpha = 0.001 \), we can see in Fig. 8 and 9, when RL is very high comparing to RS, that the efficiency is not possible because we reach nearly 100%. This is due to the fact that we neglect some components of the efficiency, the main factor is the gates charging. This effect is significant at low voltage (\( \leq 1.5V \)) because the switches and the clock buffers become very large to achieve a sufficiently low ON resistance. Note that in the above development, the RONC time-constant is assumed to be lower than 1/10fCK.

**Non-overlap switching**

At high frequency (above 1MHz), dynamic losses become important and to make things work properly we must avoid overlapping the two serial switches (M3, M4). This is done by adding asynchronous delays between the two gate signals. The same can be applied to the transistors M1, M2 (Fig. 10).
Conductance improvement

Up to now the gate signals of the two serial switches (M3, M4) were between \( V_{IN} \) and \( 2V_{IN} \). The conductance is greatly improved if these signals range between 0 and \( 2V_{IN} \). This is very important for \( V_{IN} \) under 1.5V. Assuming a \( V_{IN} \) of 1.5V and a \( V_T \) of 1V then the ON voltage is 0.5V in the proposed schematic. Driving these switches between 0 and \( 2V_{IN} \) boosts the ON voltage to 2V, thus dividing by four the ON resistance.

6. EXPERIMENTAL RESULTS

Real application often requires a few mA drive capability for the DC-DC converter. Supplying such a current requires very large capacitors (or clock frequency). Therefore external capacitors should be used. This constraint is dramatically compensated by a significant improvement on the efficiency: external capacitors give a very low \( \alpha \) (0.001) and allow a low clocking frequency, thus a low fC\text{-}V loss in the switches. For example, a voltage doubler with 100nF external capacitors and 50KHz clocking frequency gives an output resistance of 100\( \Omega \). This circuit has been implemented in a 2\( \mu \)m CMOS technology (Fig. 11).

Fig. 10: Non-overlapping gate signals

Fig. 11: Microphotograph of the voltage doubler; the chip size is 2mm x 1mm in a 2\( \mu \)m technology (capacitors are external)

Measured and calculated efficiency from equation (7) with \( \alpha = 0.001 \) are plotted in Fig. 12. We can see that our equation is no longer valid for a small output current (\( R_S/R_L \rightarrow \infty \)) because the neglected switching current becomes dominant. The total current consumption without load is 30\( \mu \)A while only 15\( \mu \)A should be lost in the stray capacitors. The 15\( \mu \)A comes both from the switches gate and the transient short-circuit current of the four stages buffer that generates CK and CK (Fig. 7).

Fig. 12: Efficiency measurement versus calculated. We can see clearly that our efficiency expression (7) well match the measures with heavy load but not for light load.

7. CONCLUSION

The feasibility of a high efficiency CMOS voltage doubler depend on the making of a good serial switch. This switch was analyzed and a model suitable for simulation was described. A solution was found for a charge pump cell and the measured circuit showed no substrate current. The efficiency of our voltage doubler is greatly improved for heavy capacitive loads. With all improvements presented here and external capacitors, an efficiency up to 94\% has been demonstrated.

The principle presented here is not restricted to doubler but can also be used for triplers and other multipliers. Two doublers can also be cascaded to reach four times the input voltage.

8. REFERENCES
