Snubberless Bidirectional DC–DC Converter With New CLLC Resonant Tank Featuring Minimized Switching Loss

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Abstract—A bidirectional dc–dc converter (BDC) with a new CLLC-type resonant tank, which features zero-voltage switching (ZVS) for the input inverting choppers and zero-current switching (ZCS) for the output rectifier switches, regardless of the direction of the power flow, is proposed in this paper. Possessing the very optimal ZVS+ZCS soft-switching feature, this proposed converter will have a minimized switching loss if all of the main switches are implemented with metal–oxide–semiconductor field-effect transistors, and thereby, the proposed converter is fully soft switched and totally snubberless. The detail operation principles, as well as the design considerations, are presented. The methodologies to develop a unidirectional ZVS+ZCS dc–dc converter for the corresponding pulsewidth modulation and frequency modulation converters are proposed. The approach on how to construct a fully soft-switched BDC has also been proposed and analyzed. Finally, a topology extension is made, and another fully soft-switched BDC is derived. A prototype, which interfaces the 400–48-V dc buses for the uninterrupted power supply system with a power rating of 500 VA, was developed to verify the validity and applicability of this proposed converter. The highest applicable conversion efficiencies for the bidirectional operational modes are exceeding 96%.

Index Terms—Bidirectional dc–dc converter (BDC), topology combination, zero-current switching (ZCS), zero-voltage switching (ZVS).

I. INTRODUCTION

W ITH THE increasing demands for electric power in future automobiles, uninterrupted power supplies (UPSs), renewable energy sources, telecom and computer systems, and aviation power systems, bidirectional dc–dc converters (BDCs) exhibit as an ever-lasting key component to interface between a high-voltage bus, where an energy generation device such as a fuel cell stack and/or a photovoltaic array is installed, and a low-voltage bus, where usually an energy storage device such as a battery or a supercapacitor is implemented, to actively provide clean and stable power and to enable high reliability, effectiveness, and maneuverability of the power systems aforementioned [1]–[13], as shown in Fig. 1. Basically, a BDC can be developed by directly replacing output rectifiers with current bidirectional active switches (which implies that the metal–oxide–semiconductor field-effect transistor (MOSFET) perhaps is the most suitable applicable device for low-to-middle power rating applications since the synchronous rectification (SR) technique is possibly feasible for upgrading the overall conversion efficiency remarkably), either using the resonant [3]–[5] or the pulsewidth modulation (PWM) [6]–[8] pattern unidirectional converters. In addition, galvanic isolation with a high-frequency transformer is often required for flexibility of system reconfiguration and meeting safety standards [9]. Nowadays, plenty of soft-switching BDCs with focus on eliminating the switching loss, reducing the electromagnetic interference, and achieving an attainable high-frequency operational ability and, thereby, power density without sacrificing the efficiency have been praised and extensively reported in the open literature [5]–[15], [16], [17]. Generally, the soft-switching techniques can be sorted as two groups: the zero-voltage-switching (ZVS) technique and the zero-current-switching (ZCS) technique. The ZVS approach is preferred for the majority of carrier semiconductor devices such as MOSFETs when being implemented as the input inverting choppers, since the turn-on loss due to energy discharging of the output capacitance is large enough. The ZCS approach is suitable for the minority of carrier semiconductor devices such as insulated-gate bipolar transistors and power diodes, since the turn-off loss is large due to the characteristic of current tail. Moreover, the MOSFETs, which are used as the output SR rectifiers, should also adopt the ZCS technique since high rectifier current will flow through the intrinsic diode of the MOSFET. Based on the two kinds of soft-switching techniques, several attempts have been proposed to try to reduce the switching loss of the BDC as much as possible. Reference [10] introduces a BDC operating in the phase-shifted manner, which can realize ZVS for the voltage-fed side switches. However, the switches on the current-fed side remain operating under hard switching conditions. In [11]–[15], several BDCs are presented, where the ZVS attribute is enabled for the switches operating in the input inverting stage, according to the power flow direction. However, in the corresponding output stage on the other side of the transformer, the rectifier switches snap off, and a high-voltage surge is observed, where the reverse-recovery loss remains unsolved and the RCDI snubbers are required [11]. To solve the reverse-recovery issue, several ZCS BDCs have been presented [16]–[18]. In these ZCS BDCs, both of the input and output stage...
switches realize ZCS regardless of the direction of the power flow, which have a significant reduction of the reverse-recovery loss for the rectifier switches. Unfortunately, the turn-on loss for the input inverting choppers is considerable, and the conversion efficiency exacerbates particularly when the BDC operates in high-voltage applications. Recently, there is growing interest in the area of soft-switching resonant topologies [19]–[30]. In [21]–[24], the conventional LLC resonant converter has been proposed and investigated to improve the overall conversion efficiency [25], since this LLC topology possesses the soft-switching feature as the ZVS for input inverting choppers and ZCS for output rectifiers. If the power switches on the primary side are all equipped with MOSFETs, the conventional LLC converter has a minimized switching loss. Whereafter, several methodologies to improve the performance of the conventional LLC converter have been proposed [26]–[28]. Furthermore, another LCC converter, which processes the same ZVS+ZCS soft-switching feature as that of the conventional LLC converter, has been proposed in [29]. However, the conventional LLC and LCC converters aforementioned are both unidirectional. If they were applied in the bidirectional applications, the operation principles would change greatly, and their soft-switching advantages would no longer be attained. Thus, the soft-switching techniques that are particularly effective for the BDC still need to be investigated. Table I concludes the criteria for the most suitable soft-switching techniques for a BDC to minimize the switching frequency, according to the power devices adopted for the input and output stages.

From Table I, it can be clearly seen that if symmetrical ZVS+ZCS soft-switching techniques could be achieved in a BDC, regardless of the direction of power flow, the switching loss can be minimized if all of the power switches are equipped with MOSFETs. With the minimized switching loss, the all-MOSFET-equipped BDC can be totally snubberless and very suitable for low-to-middle power rating applications. This paper presents such a minimized switching loss BDC. The soft-switching feature for the proposed converter is realized only by a very simple CLLC resonant tank. Without any other additional soft-switching auxiliary circuits and being snubberless, the overall component count can be dramatically reduced. Furthermore, the proposed converter has a very wide input range, which can fully exploit the energy of the storage devices as the source and lengthens its life cycle. The operation principles and design considerations of the proposed converter are described. The experimental results obtained from a 500-VA prototype are also presented to confirm the validity and applicability of the proposed converter.

II. TOPOLOGY DERIVATION AND OPERATION PRINCIPLES

The circuit configuration of the proposed converter is shown in Fig. 2, which is very similar to the conventional LLC resonant converter from the topology point of view, except for
the additional resonant capacitor $C_{S2}$. As a matter of fact, in the topology exploration contributed by Severns [19], the conventional LLC converter with the network ID of 4 (hereinafter, “Type-4”) is not the only soft-switching converter with three resonant elements that features ZVS for the input inverting choppers and ZCS for output rectifier switches when operating under the boost mode. Actually, which had not been pointed out by Severns, the kind of LLC tank of the 11th (hereinafter, “Type-11”) presented in [19] has the same soft-switching attributes as those of the Type-4 tank. As shown in Fig. 2, it is not hard to find that the Type-4 and the Type-11 resonant tanks can share both of the two inductors, $L_S$ and $L_m$, without their position relocated topologically. This inspires the idea that a novel BDC, which can combine the Type-4 and Type-11 resonant tanks together, achieves the desired soft-switching attributes of ZVS + ZCS as stated previously in Section I. As shown in Fig. 2, the resonant tank of the proposed converter originates from the combination of the Type-4 and the Type-11 resonant tanks and has been reshaped into a four-element tank of C-L-L-C, to possess such bi-directional ZVS + ZCS feature.

The proposed converter can be developed either in a full-bridge or half-bridge manner, and the magnetic inductor of the transformer is devoted to be utilized as the resonant inductor $L_m$ to realize magnetic integration. A possible topology implementation of the proposed converter has been shown in Fig. 2. Aside from the main CLLC resonant tank, the switch groups $S_1$-$S_4$ and $S_5$-$S_8$, where their intrinsic diodes and the output capacitors are appropriately shown, are constructed into the full-bridge configuration and multiused as the input inverting stage or the output rectifier stage. To avoid flux imbalance for $T_R$, the resonant capacitors $C_{S1}$ and $C_{S2}$ can also be functionalyzed as the blocking capacitors according to the present direction of the power flow.

Both directions of the power flow are modulated under the variable frequency modulation (FM) above resonance. This FM control strategy can be described separately according to the operation mode. In the modified Type-4 LLC mode (hereinafter, “MT-4 mode”), the inverting choppers $S_1$&$S_4$ and $S_2$&$S_3$ run at 50% duty cycle, 180° out of phase; the rectifier switches $S_6$&$S_7$ and $S_5$&$S_8$ are driven by the SR signals. Contrastively, in the modified Type-11 mode (hereinafter, “MT-11 mode”), the inverting switches $S_6$&$S_7$ and $S_5$&$S_8$ run at 50% duty cycle, 180° out of phase; the rectifier switches $S_1$&$S_4$ and $S_2$&$S_3$ are driven by the SR signals. The main principle waveforms for both MT-4 and MT-11 modes are shown in Fig. 3. The two operation modes have eight operation stages during a switching period. The equivalent circuits in the former four operation stages in a half switching cycle for both modes of MT-4 and MT-11 are shown in Fig. 4. Other four stages in each mode are symmetrical to those of the previous half cycle, so they are omitted here. To simplify the process of the analysis, the following are assumed.

1) The converter is under a steady operation state.
2) The dead times are lengthened on purpose for the convenience of analysis.
3) The magnetic inductor $L_m$ has an apparently much larger value of inductance, namely, three to five times, than $L_S$.

Based on the assumptions, the detailed operating processes for the MT-4 and MT-11 modes can be described detailedly in the following texts.

1) **MT-4 Mode**:

**Stage 1** [$t_0$, $t_1$]: At time $t_0$, $S_1$ and $S_4$ are conducting. The modified Type-4 resonant tank can simply be recognized as constituting the series $C_{S1}$, $L_S$, and $C_{S2}$, and the resonant current $i_{L_S}$ will increase in a sine-wave shape. The
magnetic current $i_{Lm}$ does increase but resonates much slower than $i_{Ls}$. On the secondary side, the rectified currents $i_{S6}$ and $i_{S7}$, which are carried by the SR of $S_6$ and $S_7$, are proportional to the difference between the terms $i_{Ls}$ and $i_{Lm}$.

Stage 2 $[t_1, t_2]$: When $i_{Ls}$ resonates over its peak, it begins to decline and is equal to the increasing magnetic current $i_{Lm}$ at time $t_1$. The rectifier current on the secondary side decreases to zero, and $S_6$ and $S_7$ turn off under ZCS conditions. The voltage on the resonant capacitor $C_{S2}$ also resonates to its peak with the absolute value of $V_{C_{S2}}$. It will remain unchanged unless it excites again in the next resonance. The disconnection of $C_{S2}$ with the primary side avails the free resonance between $C_{S1}$, $L_{S}$, and $L_{m}$ on the primary side.

Stage 3 $[t_2, t_3]$: At time $t_2$, $S_1$ and $S_4$ turn off. $i_{Ls}$ begins to charge the parasitic capacitance of $S_1$ and $S_4$ and discharge that of $S_2$ and $S_3$ simultaneously. Since the value of the parasitic capacitance is small compared with that of the resonant capacitor $C_{S1}$, this time period is rather short with respect to the total switching period. Thus, the corresponding voltages on the aforementioned capacitance rise/decrease rapidly. This stage ends up with $v_{ds1,4}$ reaching the input voltage and $v_{ds2,3}$ decreasing to zero. At the end of this stage, the voltage applied on the resonant tank has charged its polarity from positive $V_1$ to negative.

Stage 4 $[t_3, t_4]$: After the full discharge of $S_2$ and $S_3$, the resonant current $i_{Ls}$ immediately flows through the body diodes of $S_2$ and $S_3$ and feeds back to the input source. When the voltage of the magnetic inductor $L_m$ resonates to reach the voltage of $V_2 - V_{C_{S2}}$, the rectifier switches $S_5$ and $S_8$ conduct, and the resonant capacitor $C_{S2}$ participates the resonance with the primary side again. At time $t_4$, $S_2$ and $S_3$ turn on under ZVS conditions, the first-half switching period ends, and the converter enters the next (the second) half.

2) MT-11 Mode:

Stage 1 $[t_0, t_1]$: At time $t_0$, $S_6$ and $S_7$ are conducting. The modified Type-11 resonant tank can simply be recognized as constituting the series $C_{S2}$, $L_{S}$, and $C_{S1}$, and the resonant current $i_{C_{S2}}$ will increase in a sine-wave shape. The magnetic current $i_{Lm}$ does increase but resonates much slower than the resonant current $i_{C_{S2}}$. On the secondary side, the rectified currents $i_{S6}$ and $i_{S7}$, which are carried by the SR of $S_6$ and $S_7$, are proportional to the difference between the terms $i_{C_{S2}}$ and $i_{Lm}$.

Stage 2 $[t_1, t_2]$: When $i_{C_{S2}}$ resonates over its peak, it begins to decline and is equal to the increasing magnetic current...
$i_{Lm}$ at time $t_1$. The rectifier current on the secondary side decreases to zero, and $S_1$ and $S_4$ turn off under ZCS conditions. The voltage on the resonant capacitor $C_{S1}$ also resonates to its peak with the absolute value of $V_{C_s1}$. It will remain unchanged unless it excites again in the next resonance. The disconnection of $C_{S1}$ and $L_S$ avails the free resonance between $C_{S2}$ and $L_m$ on the primary side.

**Stage 3** [$t_2$, $t_3$]: At time $t_2$, $S_5$ and $S_7$ turn off. $i_{C_6}$ begins to charge the parasitic capacitance of $S_6$ and $S_7$ and discharge that of $S_5$ and $S_8$ simultaneously. Since the value of the parasitic capacitance is small compared with that of the resonant capacitor $C_{S2}$, this time period is rather short with respect to the total switching period. Thus, the corresponding voltages on the aforementioned capacitance rise/decrease rapidly. This stage ends up with $v_{ds6,7}$ reaching the input voltage and $v_{ds5,8}$ decreasing to zero. At the end of this stage, the voltage applied on the resonant tank has charged its polarity from positive $V_2$ to negative.

**Stage 4** [$t_3$, $t_4$]: After the full discharge of $S_5$ and $S_8$, the resonant current $i_{C_2}$ immediately flows through the body diodes of $S_5$ and $S_8$ and feeds back to the input source. When the voltage of the magnetic inductor $L_m$ resonates to the voltage of $V_1 - V_{C_s1}$, the rectifier switches $S_2$ and $S_3$ conduct, and the resonant elements on the secondary side participate the resonance with the primary side again. At time $t_4$, $S_5$ and $S_8$ turn on under ZVS conditions, the first-half switching period ends, and the converter enters the next (the second) half.

It can be comprehended that, in both of the two modes, the additional resonant capacitors $C_{S1}$ and $C_{S2}$ appear and disappear at the same time with the load, as seen from the input stages. This is almost the same operation principle with the original Type-4 and Type-11 LLC resonant tanks and gives the explanation why they both possess the same soft-switching features as the Type-4 and Type-11 LLC tanks. As a consequence, the insertion of $C_{S1}$ and $C_{S2}$ to the original Type-4 and Type-11 resonant tanks will only slightly modify the resonant frequency when all of the four resonant elements are involved, but not change the fundamental of the original resonant tanks very much.

**III. Design Considerations**

**A. Behavioral Difference for the MT-4 and MT-11 Tanks**

As having been well developed and widely known [30], [31], the original Type-4 and Type-11 LLC resonant tanks have very similar behavior over the switching frequency. They share the same amount of resonant stages in a switching cycle, have the same operation modes of leading and lagging power factor modes, and even have very similar dc gain curves. As the descents of the Type-4 and Type-11 LLC resonant tanks, the MT-4 and MT-11 resonant tanks also resemble each other in circuit characteristics. However, a slight difference of these converters presents the exact values of dc gain at the same point where the normalized switching frequency is specified. A comparison from the topology configuration point of view was made to investigate the difference in characteristics of the two resonant tanks.

From the tutorials to the in-depth technique papers, the operation principle for the original Type-4 LLC converter has been extensively considered as a band filter with the series-parallel kind of resonant tank. Coincidently but apparently, the Type-11 LLC converter can also be recognized as a series-parallel resonant tank, with the different inserting location of an extra paralleled resonant inductor developed from the original basic LC series resonant converter (SRC). However, the Type-4 LLC converter has a closer manner with the conventional LC SRC, because during the $L_S - C_S$ resonant stage, the load is in series with the resonant tank. Contrarily, the Type-11 LLC converter is much closer to the CL parallel converter, since the load is paralleled with the resonant tank during the $C_S - L_m - L_S$ resonant stage. Thus, like the difference associated with the dc gain between the parallel resonant converter (PRC) and SRC, the voltage gain of the Type-11 LLC converter is higher than that of the Type-4 LLC converter at the same point of switching frequency. This conclusion still stands even for the modified LLC resonant tank, since the extra capacitor acts like a dc blocking capacitor for both MT-4 and MT-11 modes. This conclusion can also be proved by the theoretical analysis based on the frequency domain. The equivalent frequency-domain circuits for the MT-4 and MT-11 resonant tanks are shown in Fig. 5, where $R_V$ is the equivalent load resistance.

Based on the approach of fundamental mode approximation (FMA) [32], [33], the equations of the dc gain for both MT-4 and MT-11 modes can be expressed as follows:

$$M_{MT4} = \left| \frac{(R_V + Z_{C_s2})/Z_{Lm}}{Z_{C_s1} + Z_{L_s} + (R_V + Z_{C_s2})/Z_{Lm}} \right| \cdot \frac{R_V}{|R_V + Z_{C_s2}|}$$

$$M_{MT11} = \left| \frac{(R_V + Z_{L_s} + Z_{C_s1})/Z_{Lm}}{(R_V + Z_{L_s} + Z_{C_s1})/Z_{Lm} + Z_{C_s2}} \right| \cdot \frac{R_V}{R_V + Z_{L_s} + Z_{C_s1}}$$

Define

$$Q_1 = \frac{\sqrt{L_S}}{R_V} \cdot \frac{C_{S1}}{L_S}$$

$$Q_2 = \frac{\sqrt{L_S}}{R_V} \cdot \frac{C_{S2}}{L_S}$$

$$\omega_{T_4} = \frac{1}{\sqrt{L_S \cdot C_{S1}}} \cdot \frac{\omega_S}{\omega_{T_4}}$$

$$\omega_{T_{11}} = \frac{1}{\sqrt{(L_S/L_m) \cdot C_{S2}}} \cdot \frac{\omega_S}{\omega_{T_{11}}} \cdot \sqrt{\frac{h}{1 + h}}$$

$$h = \frac{L_m}{L_S} \cdot g = \frac{C_{S2}}{C_{S1}}$$

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*Fig. 5. Equivalent circuits for forward and reverse modes. (a) DC gain curve for forward mode. (b) DC gain curve for reverse mode.*
where $\omega_S$ is the switching frequency. Then, (1) and (2) can be simplified, respectively, as

$$M_{MT4} = \left| \frac{1}{a_1 - j \cdot b_1} \right| = \frac{1}{\sqrt{a_1^2 + b_1^2}}$$  \hspace{1cm} (3)

$$M_{MT11} = \left| \frac{1}{a_2 - j \cdot b_2} \right| = \frac{1}{\sqrt{a_2^2 + b_2^2}}$$  \hspace{1cm} (4)

where

$$a_1 = \frac{1}{h} + 1 - \frac{1}{h \cdot \omega_1^2}$$

$$a_2 = 1 - \frac{1}{h \cdot \omega_2^2}$$

$$b_1 = Q_1 \cdot \left( \frac{1}{\omega_1} - \omega_1 \right) + Q_1 \cdot \frac{(1 + h)}{g \cdot h \cdot \omega_1} - \frac{Q_1}{g \cdot h \cdot \omega_1^3}$$

$$b_2 = Q_2 \cdot \left( \frac{1}{\omega_2} - \omega_2 \right) + \frac{Q_2 \cdot (1 + h \cdot g)}{h \cdot \omega_2} - \frac{Q_2}{h \cdot \omega_2^3}.$$  

According to (3) and (4), the normalized dc gain against switching frequency can be shown in Fig. 6.

From Fig. 6, it can be observed that the voltage gain curves of MT-4 and MT-11 are very similar with each other, where they both have two resonant peaks located on either side of the point-of-unity normalized switching frequency, respectively. However, the difference shows visibly in the area where the normalized switching frequencies of the two modes are both higher than unity. In this area, the voltage gain of MT-11 can be correspondingly a little higher than that of MT-4. Moreover, since the dc blocking effect exhibits in the extra capacitor for the corresponding power flows, both the dc gains of MT-4 and MT-11 modes are smaller than those of the original Type-4 and Type-11 LLC converters, due to a part of energy that has been stored in the additional capacitors. Moreover, the frequency of resonance for both two modes has not been the $\omega_{T_4}$ or $\omega_{T_{11}}$ any more, since the extra capacitor for each mode actually participates in the resonance and substantially changes the resonance frequency. Nevertheless, the new resonance frequency is by no means exact to be the frequency of $1/\sqrt{L_S \cdot (C_{S1}/C_{S2})}$. This is because the resonant inductor $L_m$ still needs some portion of energy to be excited during the stages that transfer energy to load. This separation of energy substantially interferes the full resonance for $L_S - C_{S1} - C_{S2}$.

The precise symbolic solutions for the resonance frequency of the two modes can be solved by letting the image part of (1) and (2) be zero. However, for the complexity, the expressions are omitted here.

**B. Design Procedure for the CLLC Resonant Tank**

As was analyzed previously, the voltage gains for MT-4 and MT-11 modes are not the same, and the MT-11 mode always has a higher dc gain than the MT-4 mode. Therefore, MT-11 is much more suitable for converting the power from a low- to a high-voltage bus. However, due to the difficulties when it comes to solving all of the four elements at the same time, it becomes more convenient to design firstly a basic Type-4 or Type-11 resonant tank and, lastly, cope with the last remaining resonant capacitor. To alleviate the design difficulties, it is more suitable to start firstly with the design of a Type-4 LLC resonant tank, provided the extensive research and abundant reference of the Type-4 LLC converter. Then, the design procedure can be outlined by the following eight steps.

1) Choose a proper value for resonance frequency $\omega_{T_4}$ (or $f_{T_4}$)

$$f_{T_4} = \frac{1}{2\pi\sqrt{C_{S1} \cdot L_S}}.$$  \hspace{1cm} (5)

Since the proposed converter has the symmetrical ZVS+ZCS feature, achieving the minimized switching loss when all the power switches are equipped with MOSFETs, the switching loss is therefore hardly associated with the switching frequency. A possible consideration to evaluate whether the candidate switching frequency is suitable for the application or not is by determining the size of the power supply, or the size of
the passive components to be more specific, under the selected switching frequency. The determined switching frequency should finally accommodate the desired size of the proposed converter, as required by the design specifications.

2) Parameter \( h \) should be specified as large as possible, e.g., \( h = 3 \), to accommodate a wide-input-range adaptability.

3) The inductance \( L_m \) can be determined by the optimal design methodology provided by Lu et al. [34]

\[
L_m = \frac{t_{\text{dead}}}{8 \cdot f_S \cdot C_{\text{OSS}}} \quad (6)
\]

where \( t_{\text{dead}} \) is the dead time between the upper and lower side switches in the same bridge leg, \( f_S \) is the switching frequency, and \( C_{\text{OSS}} \) is the equivalent output capacitance of the inverting switches. There is no very strict constraint for determining the dead time. However, apparently, the minimum value for the dead time should be longer enough to ensure the pair of MOSFETs in the same bridge leg can switch ON and OFF properly. To be more specific, the minimum value for the dead time should be the period of the sum of the MOSFET dynamic characteristics times as \( t_{\text{d(on)}} + t_{\text{rise}} + t_{\text{d(off)}} + t_{\text{fall}} \). However, an extremely long dead time should either be avoided. It should not be longer than the switching cycle of \( 1/f_{T-4} \), which has been determined in step 1). Basically, for the applications where the switching frequencies are in the range of several tens of kilohertz to several hundreds of kilohertz, dead time values ranging from 300 to 100 ns are empirically recommended.

4) According to (5) and (6), \( L_S, L_m, \) and \( C_{S1} \) can be determined. If the attainable maximum dc gain under this set of parameters can fulfill the requirement of the input range, then the procedure continues; otherwise, go back to step 2) to reset a new \( h \).

5) Sweep parameter \( g \) under the heaviest load of \( Q_1 \). Then, the diagram of dc gain for both MT-4 and MT-11 modes under different parameter \( g \) can be derived. Fig. 7 shows such a set of typical curves for the two modes. The appropriate choosing of parameter \( g \) highly depends on how similar the curves of the dc gain of the two modes are, under the condition of the same parameter \( g \). A proper \( g \) should make the two dc gain curves alike both in the shape and amplitude as much as possible, e.g., when \( g = 1 \), the two dc gain curves in Fig. 7(a) and (b) look alike very much. Therefore, \( g = 1 \) can be specified for proper use.

6) As parameter \( g \) having been known, the second resonant capacitor \( C_{S2} \) can be calculated by \( g = C_{S2}/C_{S1} \). Since all of the four resonant elements have been chosen, the desired curves of the dc gain against switching frequency with different load conditions can be shown in Fig. 8.
7) Check whether the dc gain can meet the variation of load and line change. If not, go back to step 6) to rechoose a more proper $g$.  
8) Determine the dc gain of the MT-4 mode at the resonance frequency from Fig. 8(a), assuming $M_{MT4-R}$. Then, the turn ratio $n$ (MT-4 mode) of the transformer can be obtained directly from

$$n = M_{MT4-R} \frac{V_{in}}{V_O}. \quad (7)$$

With $n$ being presented, the design procedure for the proposed CLLC resonant tank is completed.

C. Discussion of the Realization of the ZVS+ZCS Feature

As was pointed out in the beginning of this paper, for the dc–dc converters, whether unidirectional or bidirectional type, where the MOSFETs are implemented, the minimized switching loss essentially relies on the ZVS+ZCS feature, as the ZVS for the inverting choppers and ZCS for the rectifier switches. However, obviously, not every converter, modulated either by PWM or FM, has the ability to realize the desired ZVS+ZCS attribute. Thus, it is very meaningful to investigate and analyze the characteristics of the converters with the ZVS+ZCS feature. The breakthrough can firstly be made in the area of unidirectional dc–dc converters. After reviewing the kinds of soft-switching unidirectional dc–dc converters, it can be concluded that there are two relatively easy ways to implement the ZVS+ZCS feature, which thereby can be sorted into two groups for analysis.

Firstly, for the PWM converters, the ZVS for inverting choppers can be realized by various approaches [35]–[37], but the ZCS for the rectifier switch should be implemented by operating the converter in discontinuous current mode (DCM) mode, where the filter inductor current can naturally decrease to zero and alleviate the reverse recovery for the rectifier switches. However, since the DCM mode is not very suitable for high-power-rating applications, the PWM converters with ZVS+ZCS feature are not used widely, except for some interleaving applications.

Secondly, for the FM converters, the ZVS feature for the inverting choppers can be achieved very easily if the converter operates under the lagging power factor mode, and the ZCS feature for the rectifier switches can also be achieved if there is no bulky filter inductor at the output stage. Thus, it will be much easier to realize ZCS for the rectifier switches in the SRC than in the PRC. Taking the conventional LC SRC for example, it realized ZVS for the inverting choppers naturally when operated under the lagging power factor mode. It can also be recognized achieving ZCS for the rectifier switches (diodes) since the conducting current flowing through the rectifier (diode) resonates to zero (a relatively low $di/dt$ compared with the hard switching). Therefore, the converters, which are derived from the LC SRC, will obviously inherit the ZVS+ZCS feature, such as the Type-4 and Type-11 LLC resonant converters having. Considering that the resonant converters are suitable for most applications except for very low power rating, the resonant converters without the output filter inductor may be the best candidate for the minimized switching loss converter.

As for the BDC, apparently, the combination of two ZVS+ZCS resonant tanks together is generally the most straightforward way to have a minimized switching loss BDC for either direction of power flow. That is exactly the very original idea where the proposed converter comes from. However, during the process, when such a resonant tank is constructed, cautions should be paid on the effectiveness of the combined resonant tanks. Usually, the insertion of an extra resonant element will have influence on the characteristics of the original resonant tank. Therefore, it is not guaranteed that the combined resonant tanks will keep the desired operational principles. Moreover, the amount of the components used in the resonant tank should also be taken into account. An excellent resonant tank should keep its internal resonant elements as simple as possible and have the ability of being integrated as much as possible. The Type-4 LLC resonant converter shows a good example to illustrate how a resonant tank with such merits mentioned earlier prevails in industry.

D. Topology Extension

Two Type-4 LLC resonant tanks can also be combined and create a new resonant tank with the ZVS+ZCS feature. However, the circuit configuration of the combinatorial resonant tank with the two Type-4 LLC resonant tanks must apply with the magnetic integration technique, as shown in Fig. 9. The leakage inductance between the primary and secondary windings functions as the resonant inductor for the corresponding power flow directions. Consequently, this resonant tank operates with principles of the Type-4 LLC resonant tank in both power flow directions. However, due to the voltage gain loss analyzed in the design procedure in Section III-A, the tune of the transformer ratio can hardly compensate the converter to equalize the dc gain for bidirectional operations. Thus, the input/output specifications for this particular BDC possibly should slightly adjust to meet the change of the dc gain.
IV. EXPERIMENTAL RESULTS

A 500-VA prototype, which can be employed for the UPS system to interface the 400- and 48-V dc buses and adopts the proposed bidirectional ZVS+ZCS resonant tank, verifies its operation principle and the attribute of soft switching. The specification and main parameters are specified as follows.

1) Forward mode

\[ V_1 : 200 - 400 \text{ Vdc}; \quad V_2 : 48 \text{ Vdc}; \quad I_O : 0 - 10 \text{ A}. \]
2) Reverse mode

\[ V_2 : 24–48 \text{ Vdc}; \quad V_1 : 400 \text{ Vdc}; \quad I_O : 0–1.2 \text{ A}. \]

The components of the power stage shown in Fig. 2 are listed as follows.

High-voltage-fed side switches, \( S_1–S_4 \) : 2SK3934.
Low-voltage-fed side switches, \( S_5–S_8 \) : IPP070N08N3.
\( T_R \) : \( n \) = 35.5.
\( L_m \) : 228 \( \mu \text{H} \).
\( L_S \) : 76 \( \mu \text{H} \).
\( C_{S1} \) : 33 nF/630 V.
\( C_{S2} \) : 1410 nF (three 470 nF caps. in parallel, \( g \approx 0.9 \)).

As a consideration of the compatibility of control schemes for the two operational modes, a DSP-based digital control platform presented by Hu et al. [38] is adopted to generate the driving signals for both the high-voltage-side and low-voltage-side MOSFETs, which is shown in Fig. 10. Two current transformers, \( CT_F \) and \( CT_R \), are adopted and inserted into the proposed CLLC resonant tank to properly derive the corresponding SR driving signals. In forward mode, the digital platform commands the high-voltage-side MOSFETs operating at the desired switching frequency, under 50% duty cycle for each bridge, and determines when the low-voltage-side SR should be on and off, by monitoring the current transferred by \( CT_F \). In reverse mode, the digital platform works contrarily to give the 50% duty cycle driving signals to the low-voltage-side MOSFETs and also drives the high-voltage-side SR based on the signal sensed by \( CT_R \).

Operation waveforms for the forward mode of full load under 200- and 400-V inputs are shown in Fig. 11. Fig. 11(a) and (b) shows the ZVS feature of \( S_2 \), where it can be observed \( i_{ds2} \) is negative before the arrival of its driving signal. This negative \( i_{ds2} \) ensures \( v_{ds2} \) decreasing to zero before the switch turning on and achieving ZVS. Fig. 11(c) and (d) shows the waveforms obtained from the MT-4 resonant tank. It can be comprehended that the extra resonant capacitor \( C_{S2} \) resonates with the other three resonant elements during the stages with powering load but separates from the primary resonant tank when the current of the secondary side decreases to zero. Furthermore, it can be appreciated that the platform of the peak value of \( v_{C_{S2}} \) decreases oppositely to the increase of the switching frequency; however, the resonant period for \( C_{S2} \) remains almost the same. Fig. 11(e) and (f) shows the relationship between the transformer and the output stage rectifier switches. Since the conducting current \( i_{ds6} \) can resonate to zero at a relatively low \( di/dt \), therefore the rectifier switches (SR) realize ZCS turnoff; no reverse-recovery current can be observed, where the voltage stress of the SR switches is exactly the output voltage \( V_2 \). As a conclusion, the experimental waveforms of the MT-4 resonant tank verify the operation principles as it was desired.

The operation waveforms for the reverse mode are also shown in Fig. 11(g)–(l). Since the similarity of the waveforms for the forward mode, which consist of the ZVS, ZCS, and resonant status, can be comprehended, the details of the reverse mode are omitted here. A simple way to appreciate these waveforms for the MT-11 resonant tank is just to consider the power flows through the MT-4 resonant tank backward.

The voltage ringings on the SR, which can be seen in the SR voltage stress waveforms for both forward and reverse modes, are caused by the resonance between the inductor \( L_S \) and the parasitic capacitance of the SR, coupled by the parasitic capacitance of the transformer. Although the voltage ringings can be clearly identified, the resonance energy is much lower than expected as can be proved by the very small current fluctuation presented by the resonant currents \( i_{ds}, i_{CS2} \). Thus, this resonance can hardly degrade the converter efficiency. To suppress the voltage ringing, a possible way is to parallel the additional capacitance to the SR, considering that it is impossible to completely remove the parasitic capacitance of the transformer to decouple the resonance. However, due to the two-mode bidirectional operation principles, paralleling the additional capacitance to the SR in one mode will eventually deteriorate the ZVS condition for the same MOSFET when it operates in the other mode. Thus, a tradeoff must be taken into account. For this prototype, it is shown that all of the MOSFETs with their own parasitic capacitance have the acceptable experimental results, but it does not imply that further optimization should be restricted for performance improvement.

Fig. 12 shows the conversion efficiency for both forward and reverse modes under all conditions. The highest efficiencies for the two modes exceed 96% under a high line input. Fig. 13 shows the switching frequency versus load under a different voltage input. For the forward mode, the switching frequency varies from 65.2 to 163.7 kHz. For the reverse mode, the switching frequency varies from 73.7 to 131.1 kHz.

Fig. 14 shows the voltage gain comparison with the FMA design, time-domain state-variable design, and the measured results from the prototype, under full-load condition. It indicates that the voltage gain calculated based on the frequency-domain
FMA methodology always limits the converter to be fully exploited due to the sinusoidal assumption. As an evidence, it can be appreciated that the prototype with parameters calculated by FMA has voltage gain boost by an error range of 0%–7.6%, given the measured voltage gain curves marked with symbol “+.” The accuracy can be compensated by the time-domain state-variable approaches [39]–[41], shown by the curves with dotted lines. However, although the accuracy can be improved, the state-variable approaches are considerably time consuming for solving the multielement resonant tanks and thereby not suitable for the applied design. Thus, the high-speed FMA method is particularly attractive for this case and can design the proposed converter rapidly with relatively high precision.

Moreover, it should be noted that the measured results will never meet the state-variable results accounting for the power loss exhibiting as the voltage drop on the power devices.

V. CONCLUSION

The new BDC proposed in this paper, which has a combinatorial LLC resonant tank, possesses the optimal soft-switching features as ZVS for the inverting stage choppers and ZCS for the rectifier switches at the same time, viz., the ZVS+ZCS feature, regardless of the direction of the power flows. Thus, if the MOSFETs are implemented as the main switches, the proposed converter has the minimized switching loss and is totally snubberless. The operation principles and design procedure of the proposed converter have been analyzed and depicted. Then, analysis of the unidirectional PWM and FM converters which can possess the ZVS+ZCS feature is made, and the methodology to construct a minimized switching loss BDC is described. Finally, the experimental results verify the theoretical analysis and the merits of the proposed converter. Therefore, the proposed converter provides designers with an alternative choice for wide input range, high efficiency, and high power density bidirectional dc–dc conversion applications in industry.

REFERENCES
