Ultra-Compact High-Linearity High-Power Fully Integrated DC–20-GHz 0.18-μm CMOS T/R Switch

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Abstract—A fully integrated ultra-broadband transmit/receive (T/R) switch has been developed using nMOS transistors with a deep n-well in a standard 0.18-μm CMOS process, and demonstrates unprecedented insertion loss, isolation, power handling, and linearity. The new CMOS T/R switch exploits pattern-ground-shield on-chip inductors together with MOSFET’s parasitic capacitances to synthesize artificial transmission lines, which result in low insertion loss over an extremely wide bandwidth. Negative bias to the bulk or positive bias to the drain of the MOSFET devices with floating bulk is used to reduce effects of the parasitic diodes, leading to enhanced linearity and power handling for the switch. Within dc–10, 10–18, and 18–20 GHz, the developed CMOS T/R switch exhibits insertion loss of less than 0.7, 1.0, and 2.5 dB and isolation between 32–60, 25–32, and 25–27 dB, respectively. The measured 1-dB power compression point and input third-order intercept point reach as high as 26.2 and 41 dBm, respectively. The new CMOS T/R switch has a die area of only 230 μm × 250 μm. The achieved ultra-broadband performance and high power-handling capability, approaching those achieved in GaAs-based T/R switches, along with the full-integration ability confirm the usefulness of switches in CMOS technology, and demonstrate their great potential for many broadband CMOS radar and communication applications.

Index Terms—Broadband communications, broadband radar, CMOS switch, CMOS transmit/receive (T/R) switch, linearity, on-chip inductor, power handling, RF integrated circuit (RF IC), ultra-wideband (UWB) communications, UWB radar.

I. INTRODUCTION

TRANSMIT/RECEIVE (T/R) switches are one of the key building blocks in radar and communication systems and their ability to fully integrate with other circuits and operate over very wide bandwidths is needed to enable wideband systems on chip. Most high-performance RF integrated-circuit (RF IC) switches have been implemented in GaAs processes, especially those having bandwidths of multigigahertz and high power-handling capabilities [1]. Silicon-based CMOS technology has fast become one of the most favorable processes for RF ICs due to its low cost and highly integrative capacity. Owing to low mobility, high substrate conductivity, low breakdown voltage, and various parasitic parameters of CMOS processes, it is very challenging to design CMOS switches to achieve low-insertion loss, high isolation, wide bandwidth, and high power handling comparable to their GaAs counterparts [2]. Various CMOS T/R switches have been developed at different frequencies within 900 MHz to 15 GHz [2]–[9]. Fully integrated CMOS T/R switches operating over extremely wide bandwidths up to tens of gigahertz with high linearity and power handling have not yet been reported. As the bandwidths of radar and communication systems are pushed wider or required to cover multibands to address newly emerging applications, the need of these ultra-wideband (UWB) CMOS T/R switches becomes more critical.

In CMOS switches, the parasitic capacitances in MOSFETs limit the upper operating frequency and, hence, bandwidth. A 0.25-μm CMOS T/R switch operating from 0.45 MHz to 13 GHz has been developed based on synthetic transmission lines implemented using an on-chip coplanar waveguide (CPW) together with the MOSFETs’ capacitances [7]. This T/R switch, however, exhibits insertion loss not as good as its GaAs counterparts due to the high loss of CPW realized on the conductive silicon substrate and the loss associated with the MOSFETs. CMOS switches normally have low power-handling capability as compared to their GaAs counterparts due to low breakdown voltages and parasitic diodes existing underneath the drain and source of the MOSFET structure [3], [4]. Floating bulk was used in [4], [5], and [9] to keep the parasitic diodes from being forward biased under large input signals, hence, improving the linearity and power handling of CMOS T/R switches. An input 1-dB power compression point, i.e., $P_{1dB}$, of 21 dBm was achieved with a series-shunt topology by resistively floating the bodies of the transistors [5], [9]. A 28-dBm $P_{1dB}$ was obtained using a series MOSFET with the bulk floated by an LC tuned network for narrowband applications [4]. The power handling was also improved using an impedance transformer network (ITN) implemented using an external [3] and on-chip [6] LC matching networks. The LC matching network, however, limits the switch’s operating bandwidth due to its relatively strong frequency dependence. Moreover, the ITN causes relatively high insertion loss even though external high-Q components are used [3].

In this paper, we report on the development of a UWB fully integrated T/R switch, fabricated on a commercial standard 0.18-μm CMOS process, with unprecedented performance. The new T/R switch employs an ultra-broadband topology...
based on the synthetic transmission-line concept with on-chip spiral inductors. Simultaneously floating and applying negative bias to the bulk or positive bias to the drain are implemented to enhance the linearity and power handling of the switch. The developed CMOS T/R switch exhibits an insertion loss lower than 1 dB from dc to 18 GHz and less than 2.5 dB up to 20 GHz. The measured isolation is between 32–60, 25–32, and 25–27 dB and $P_{1\text{dB}}$ varies between 25.4–26.2, 22.6–25.4, and 19.8–22.6 dBm from dc–10, 10–18, and 18–20 GHz, respectively. The measured input third-order intercept point (IIP3) reaches as high as 41 dBm. The switch occupies a very small die area of $230\ \mu m \times 250\ \mu m$.

II. CMOS DEVICE AND BROADBAND ENHANCED POWER-LINEARITY T/R SWITCH TOPOLOGIES

A. CMOS Device With Deep n-Well and Floating Bulk

The developed CMOS T/R switch is implemented using nMOS transistors with deep n-type well (DNW). Fig. 1 shows a simplified geometry of these nMOS transistors with the gate biased so that the devices are operated under the on-state. The DNW separates the bulk of the nMOS transistors from the p-substrate. The p-n junctions between the p-bulk and n+ regions form a pair of parasitic drain-bulk (or drain) and source-bulk (or source) diodes. With DNW, large resistors can be applied directly to the bulk of nMOS devices, making it floating at high frequencies without latch-up problems that would result in RF ICs consisting of both nMOS and pMOS without DNW. Using DNW thus allows the CMOS T/R switch to be fully integrated with other RF ICs designed using both nMOS and pMOS transistors in a single chip.

Floating the bulk forces, the bulk resistances underneath the source and drain junctions open with respect to the ground, leading to a much smaller resistive loss in the conductive p-bulk than with the bulk grounded. Fig. 2 shows simplified small-signal equivalent-circuit models for the on- and off-states of floating-bulk MOSFETs when the gate is floated with a large resistor. $R_{kb}$ represents the resistive loss in the p-bulk between the source and drain. Using large gatewidths for 0.18-$\mu$m CMOS devices can produce $R_{kb}$ within several ohms, thereby resulting in low loss in the bulk. $C_{gs}$ and $C_{gd1}$ represent the gate–source and gate–drain capacitances due to the overlapping between the gate and diffusion areas. $C_{gb2}$ represents the gate–bulk capacitance. $C_{db}$ and $C_{sb}$ are the junction capacitances between the drain–bulk and source–bulk, respectively. $C_{rb1}$ and $C_{rb2}$ in Fig. 2(a) represent the distributed capacitances between the inversion layer and bulk. $C_{db}$ in Fig. 2(b) is the source–drain diffusion capacitance in a multifinger MOSFET. All these parasitic capacitances are on the order of tens of femtofarads for 0.18-$\mu$m CMOS devices and increase with the device’s gatewidth.

B. CMOS T/R Switch Topologies

The series-shunt T/R switch with two identical arms is perhaps the most commonly used topology. In this topology, the series and shunt MOSFETs dominate the insertion loss and isolation, respectively. Low insertion loss and high isolation may be achieved by using properly compromised large devices due to their small on-state resistances, which are scaled down approximately as $L/W$ with “L” and “W” denoting the gate length and gatewidth, respectively, in advanced submicrometer CMOS processes. Large devices, however, have significant parasitic capacitances, causing considerable effects to circuit matching and eventually limiting the switch’s bandwidth—especially in the high-frequency regions. These parasitic capacitances are much more pronounced in submicrometer CMOS processes. In practical switching circuits, the effects of parasitic capacitances are much more severe than the on-resistances in large submicrometer CMOS devices, particularly at high frequencies.

Synthetic transmission lines can be used to alleviate the bandwidth limitation in CMOS T/R switches. A synthetic transmission line can be created by cascading multiple sections of an identical series inductor and shunt capacitor, whose inductance and capacitance can be properly chosen to realize a particular characteristic impedance and velocity. Such a synthetic transmission line approximates a transmission line over a finite bandpass. The characteristic impedance $Z_0$ and cutoff frequency $f_c$ of an ideal lossless synthetic transmission line can be approximated as

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

and

$$f_c = \frac{1}{\pi \sqrt{LC}} = \frac{1}{\pi Z_0 C} \tag{2}$$

where $L$ and $C$ represent the inductance and capacitance of the series inductor and shunt capacitor, respectively. The cutoff frequency is thus determined, for given characteristic impedance, by the shunt capacitance.
Fig. 3 shows the topologies of the developed CMOS T/R switch. These topologies are identical, except for different bias schemes for the shunt transistors [bulk bias in Fig. 3(a) and drain bias in Fig. 3(b)], used to enhance the switch’s linearity and power handling, which will be discussed in Section II-C, and can be implemented using the same switch. Synthetic transmission lines, realized using two series ($M_1$ and $M_2$) and two shunt ($M_3$ and $M_4$) nMOS transistors, and three series on-chip spiral inductors ($L_1$, $L_2$, and $L_3$) are used to achieve a very wide bandwidth. The bias resistors ($R_{G1}$, $R_{G2}$, $R_{G3}$, $R_{G4}$, $R_{D1}$, and $R_{D2}$) have large resistances in order to isolate the dc-bias voltages from the RF signals. Large bulk resistors ($R_{B1}$, $R_{B2}$, $R_{B3}$, and $R_{B4}$) are used to make the transistors floating at high frequencies to reduce the substrate loss and increase the switch’s linearity and power-handling capability. Large series and shunt nMOS transistors with gatewidths in the order of several hundred micrometers are used to obtain small on-resistances and, hence, low insertion loss and high isolation for the switch, besides enhancing the linearity and power-handling capability. These devices, although much larger than those used in recently published CMOS T/R switches [5], [6], [8], and [9], still result in extremely wide bandwidth due to the use of the synthetic transmission-line technique.

Fig. 4(a) and (b) shows the simplified small-signal equivalent-circuit models of the MOSFETs under on and off conditions deduced from Fig. 2(a) and (b), respectively. The on-model includes the on-resistance $R_{on}$ in parallel with the on-capacitance $C_{on}$, which represents the total capacitance $C_g$ seen at the gate consisting of $C_{gb}$, $C_{g1}$, and $C_{gs}$ in Fig. 2(a), the on-state bulk capacitance $C_{b1}$ consisting of $C_{db}$, $C_{sb}$, $C_{rb1}$, and $C_{rb2}$ in Fig. 2(a), and the drain–source capacitance $R_{ds}$. The off-model is represented by the off-capacitor $C_{off}$, which consists of the total capacitance $C_{g}$ seen at the gate consisting of $C_{gb}$, $C_{g1}$, and $C_{gs}$ in Fig. 2(b), the off-state bulk capacitance $C_{b2}$ consisting of $C_{db}$ and $C_{sb}$ in Fig. 2(b), the drain–source capacitance $C_{ds}$, and the drain–source resistance $R_{ds}$. Fig. 4(c) shows the small-signal equivalent circuit of the on-path between the ANT and RX ports, where $C_{off}$ represents the combined off-capacitances $C_{off-M1}$ of $M_1$ and $C_{off-M4}$ of $M_1$, and $R_{on-M3}$.

C. Linearity and Power-Handling Enhancement

Typical CMOS switches have poor linearity and power handling, primarily due to the resultant forward bias of the drain and source parasitic diodes under operation, even with small transient voltage swings. In order to overcome the forward-bias problem and, hence, increasing the switch’s linearity and power-handling capability, the bulk can be floated and negatively biased simultaneously, as shown in Fig. 3(a). Due to small on-resistance of the series MOSFETs, the source and drain are kept approximately at the same potential under the on-state. The parasitic drain and source diodes are thus always kept reverse biased even when there are strong voltage swings at the drain and source, respectively. However, because the sources of the shunt MOSFETs are grounded, a negative voltage swing on the drain can push the two back-to-back parasitic diodes into a forward-bias region. Consequently, the voltage on the drain is clamped to a certain value in the negative region by these forward-biased diodes, leading to distortion in the output signal and, consequently, degrading the insertion loss, linearity, and power handling.

Fig. 5 illustrates three conditions for a shunt MOSFET, which result in different linearity and power-handling capabilities. In Fig. 5(a), the bulk of the MOSFET is grounded directly. When the RF voltage swing at the drain is lower than $-2V_{B}$, where $V_{B}$ is the forward pinch-on voltage of the parasitic diodes, the
back-to-back parasitic diodes are all forward biased and, consequently, the MOSFET functions as a small forward-biased resistor in parallel with the capacitor $C_{\text{off}}$. The output voltage of the switch is then approximately clamped to $-2V_B$. Fig. 5(b) shows the MOSFET with the bulk floated through a grounded resistor. A voltage swing reaching $-V_B$ at the drain would push the drain parasitic diode forward biased, but the large resistor at the bulk keeps a high impedance between the drain and ground and the source parasitic diode reverse biased, thus improving the power-handling capability. It was reported that the 1-dB compression point $P_{1,\text{dB}}$ is improved by 2 dB using this technique [5]. Fig. 5(c) demonstrates a new technique to further improve linearity and power handling. It shows the floating bulk of the shunt MOSFET is biased using a negative dc voltage via the bulk bias resistor $R_B$. This technique is implemented in the topology shown in Fig. 3(a). Since there is no current flow through $R_B$, the dc potential of the bulk node is kept the same as the negative bias. Therefore, the source parasitic diode is always in the reverse bias and the drain parasitic diode can withstand a strong negative voltage swing to $-V_B$. Using the negative bulk-bias technique can, therefore, lead to larger power handling for CMOS switches than the other two methods shown in Fig. 5(a) and (b). It is noted that, due to no output current required for the negative voltage source, a negative voltage reference can be implemented in fully integrated systems without any noise and stability issues.

The linearity and power-handling capability can also be improved by generating a positive dc potential between the drain and bulk of the shunt MOSFETs. This is achieved by applying a positive bias to the drain of the shunt MOSFETs and grounding the bulk resistors, as seen in the topology shown in Fig. 3(b). This positive-drain bias technique is especially attractive when the RF signal entering the receiver or leaving the transmitter port has a positive dc offset because no dc blocks would be needed, thus making it very useful for integration with other RF ICs in a single chip. Using the same CMOS T/R switch, both the negative-bulk and positive-drain bias techniques give the same measured results for linearity and power handling.

### III. CMOS Switch Design and Fabrication

The CMOS T/R switch was designed and fabricated using the TSMC 0.18-μm CMOS triple-well process [10] with nMOS transistors and on-chip spiral inductors. On-chip inductors in silicon-based RF ICs contribute considerable insertion loss and size because of their limited quality ($Q$) factor and relatively large size. To achieve a very low insertion loss for the switch, the total resistance of the switch’s on-path, consisting of both on-resistances of the MOSFETs and self-resistances of the on-chip inductors, needs to be designed to be as small as possible. These on-chip inductors were designed using patterned ground shields (PGSs) implemented on the polysilicon layer [11]. PGS implemented on a polysilicon layer gives higher $Q$ than that using a metal layer due to its relatively low conductivity, which results in less eddy currents. The PGS underneath each spiral prevents or partly prevents the electric fields generated by the current flowing along the spiral from penetrating into the lossy silicon substrate. This not only results in significantly reduced coupling between on-chip inductors through the substrate, but also electrical loss due to the substrate, particularly at high frequencies [12]. On-chip spiral inductors with PGS can, therefore, have high $Q$ and be located close to each other while keeping sufficient isolation between them, effectively resulting in very low insertion loss and small die area for the switch.
Fig. 7. Microphotograph of the CMOS T/R switch. The die area without pads is 0.06 mm².

Fig. 8. Measured and calculated: (a) insertion loss and isolation and (b) return loss at the antenna and TX/RX ports.

![Graph](image)

**Fig. 8.** Measured and calculated: (a) insertion loss and isolation and (b) return loss at the antenna \( S_{11} \) and TX/RX \( S_{22} \) ports.

Fig. 9. (a) Measured IIP3 at 5.8 GHz and (b) \( P_{1dB} \) with 0- and \(-1.8\) V bulk bias voltage.

![Graph](image)

**Fig. 9.** (a) Measured IIP3 at 5.8 GHz and (b) \( P_{1dB} \) with 0- and \(-1.8\) V bulk bias voltage.

Fig. 6 compares the \( Q \) of the designed 1.5-turn spirals with and without PGS calculated using the electromagnetic (EM) simulator IE3D [13]. The \( Q \) was determined using \( Q = \frac{\text{Re}(Z_{\text{in}})}{|\text{Im}(Z_{\text{in}})|} \), where \( Z_{\text{in}} \) is the input impedance of the lumped-element \( p \) equivalent-circuit model of the spiral with one port grounded. As can be seen, the \( Q \) of the PGS inductor is improved up to approximately 37 GHz with a maximum around 20 GHz. The PGS spiral has approximately 0.85-Ω series resistance below 5 GHz and about 1.67 Ω at 20 GHz.

Several remarks need to be made at this point concerning the CMOS T/R switch design. As implied in (2), small transistors should be employed to achieve a wide bandwidth for the switch. On the other hand, large series and shunt devices are needed to produce low insertion loss and high isolation, respectively. A tradeoff is thus needed not only in the switch topology, but also in the device size in order to achieve simultaneously an ultra-wide bandwidth along with low insertion loss and high isolation. Particularly for the selected T/R switch topology, the inductance and \( Q \) of the on-chip spirals versus frequency should be optimized together with \( C_{\text{slant}} \), the combined off-capacitances of the series and shunt devices. The spiral inductance and \( C_{\text{slant}} \) dictate the bandwidth, while the \( Q \) affects the insertion loss.

Table I lists the parameters of the designed CMOS T/R switch. All the bias resistors are realized on the polysilicon layer to achieve small layouts. The on-resistance \( R_{\text{on}} \) is approximately 4 and 11 Ω for the employed series and shunt n field-effect transistor (nFET), respectively. The combined off-capacitance of the series and shunt nFETs is approximately 280 fF.

Fig. 7 shows a micrograph of the CMOS T/R switch, including on-wafer RF and dc probe pads, with the TX port terminated by an on-chip 50-Ω resistor. The actual area of the switch is measured only 230 × 250 μm², with the inductors occupying approximately 60% of the chip area.

**IV. CMOS T/R Switch Performance**

Measurements were conducted on-wafer using a probe station, vector network analyzer, and frequency synthesizers. Cali-
A. S-Parameter Measurement

Fig. 8 shows the measured and calculated insertion loss, isolation, and return loss of the developed CMOS T/R switch. It exhibits insertion losses of less than 0.7, 1, and 2.5 dB from dc to 10, 10 to 18, and 18 to 20 GHz, respectively. The measured isolation varies from 32 to 60, 25 to 32, and 25 to 27 dB between dc–10, 10–18, and 18–20 GHz, respectively. The measured return losses at the antenna and receiver/transmitter ports are better than 15 and 10 dB from dc to 10 GHz and 10 to 18 GHz, respectively. These results are the same for the three different bias conditions listed in Table I. As can be seen in Fig. 8(a), the measured and calculated insertion losses agree very well to approximately 18 GHz, beyond which the measured insertion loss significantly drops below the simulated result. This discrepancy above 18 GHz has been observed in several chips and is mainly caused by the inaccuracy of the transistor’s available model. We believe that this inaccuracy is due to the parameters of the model, which characterize the silicon substrate loss. The employed transistor model also leads to the discrepancy between the measured and simulated isolation and return loss seen in Fig. 8.

B. IIP3 and $P_{\text{1 dB}}$ Measurement

Fig. 9 shows the measured IIP3 ($I_{\text{IP3}}$) versus bulk bias voltage at 5.8 GHz and 1-dB power compression ($P_{\text{1 dB}}$) versus frequency. Since the available large-signal model for the transistors lacks the accuracy when the nFETs are operated at zero source to drain potential with strong voltage swings at the drain, only the measured linearity and power-handling performance are presented. As can be seen in Fig. 9(a), IIP3 can reach as much as 41 dBm by increasing the negative bias voltage. The $P_{\text{1 dB}}$ measurement was performed without bulk bias (bulk bias resistor is grounded) and with bulk bias at $-1.8$ V. The $P_{\text{1 dB}}$ with the bulk biased is more than 25 and 20 dBm from 1 to 11.5 and 11.5 to 19 GHz, respectively, reaching 26.2 dBm at around 4 GHz. It is seen that by applying a negative bias to the bulk, the power-handling capability of the switch is increased by approximately 4 dB. Similar performance for IIP3 and $P_{\text{1 dB}}$ were also obtained when the drain was biased with a positive voltage, as discussed in Section II-C.

C. Comparison to Other CMOS T/R Switches

Table II compares the performance of the developed CMOS T/R switch with those recently published. The new switch demonstrates the widest bandwidth, highest frequency, lowest insertion loss, highest isolation, and strongest power handling among the integrated series-shunt CMOS switches [2], [5], [6], [8], and [9]. It also shows wider bandwidth, higher frequency, lower insertion loss, and higher isolation as compared to the series CMOS switch [4]. Moreover, the measured IIP3 is highest among those reported [2], [3], [6], [8], and [9]. The developed switch is also the first fully integrated CMOS T/R switch providing very low insertion loss (below 0.7 dB) for UWB communication systems covering 3.1–10.6 GHz.

V. Conclusion

A new fully integrated 0.18-μm CMOS T/R switch has been developed with unprecedented performance. The developed CMOS T/R switch represents the first CMOS switch implementing on-chip spiral inductors with PGs to simulate transmission lines for ultra-broadband performance with miniaturization and simultaneously floating the bulk with negative bulk or positive drain bias to achieve high linearity and power-handling capability. These broadband and high-linearity/power-handling techniques can also be utilized for other kinds of CMOS switches. The developed CMOS T/R switch with a die area less than 0.06 mm$^2$, less than 0.7-dB insertion loss, and more than 20-dB return loss and 30-dB isolation from 3.1 to 10.6 GHz also particularly provides the best T/R switch to date for the emerging UWB wireless communication systems operating over that frequency range. The developed CMOS T/R switch with its full integration feature paves the way for full-integration into a complete CMOS system-on-chip.

### Table II

<table>
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<th>Reference</th>
<th>Technology</th>
<th>Topology</th>
<th>Frequency (GHz)</th>
<th>Loss (dB)</th>
<th>Isolation (dB)</th>
<th>$P_{\text{1 dB}}$ (dBm)</th>
<th>IIP3 (dBm)</th>
<th>Actual Chip Size (mm$^2$)</th>
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<td>26.3</td>
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