High Efficiency Isolated Half-Bridge Gate Driver with PCB Integrated Transformer

Stefan Zeltner, Fraunhofer Institute of Integrated Systems and Device Technology, Germany

Abstract

This paper describes in detail a novel concept for isolated gate drivers by combining the advantages of printed circuit board (PCB) integrated transformers with the high efficiency of a resonance driven voltage clamped gate drive circuit. The pros and cons of PCB integrated transformers in gate drive applications are discussed. The used resonance driven voltage clamped gate drive circuit is analyzed, the efficiency of the driver circuit is calculated and compared with the measured one. Overall measurements on the developed half-bridge driver prototype are presented and principle limitations are discussed.

1 Introduction

The most popular and also most common method for driving the gate of a MOSFET or an IGBT is using a voltage source with a gate resistor. Unfortunately this method suffers from poor efficiency. In fact, the whole driving energy is lost heating up the gate resistors or the driver IC. Especially in ultra high power density systems like automotive power train DC/DC converters, the gate drive circuit must be minimized in size and moreover must be highly efficient due to operating temperatures up to 125°C. In order to meet these requirements the area of the gate drive circuit should not be larger than that of the corresponding power semiconductor substrate and the height as flat as possible [1]. Furthermore, the raise of temperature above ambient temperature should not exceed approximately 30 Kelvin.

By using a voltage clamped resonance gate drive circuit with the capability to recover the energy stored in the gate capacitance, a much higher efficiency can be reached [2]. In this case even a printed circuit board integrated transformer with a relatively high winding resistance [3-4] can cover the losses while an equivalent gate drive power of 1 to 2 watt is provided. There is no need for an additional power supply regulation or for cooling the gate drive circuit. Minimized space requirements can be achieved by combining a small and simple power supply unit with a very flat PCB integrated transformer. In contrast to other proposed resonance driven gate drive circuits [5-7] the whole driving energy for turning on the power switch is stored in an inductor. The turn-off time can be adapted to reduce undesirable turn-off overvoltages through parasitic inductances while the turn-on time can be made faster independently.

1.1 Isolated Gate Drive Requirements

To cover all the aspects mentioned in the introduction the gate driver should meet the following requirements:

- Equivalent gate drive power up to 2 watt
- High galvanic isolation up to 1200 volt for the bottom and the top switch driver
- Switching frequency \( f_s \) up to 500 kHz
- Continuous on and off time capability
- Thickness less than 5 mm
- Useable up to 125°C ambient temperature

2 PCB Integrated Transformers

First of all the advantages and limitations of PCB integrated transformers based on standard FR-4 printed circuit board material with 35 \( \mu \)m copper are discussed.

2.1 Advantages

By using the copper layers of a PCB for the windings and due to the high isolation strength of the FR-4 material it is possible to realize very thin galvanic isolated transformers with two or more galvanic isolated windings. Figure 1 shows, for example, the design of a 2 mm thick transformer which supplies both galvanic isolated secondary sides of the developed half-bridge gate driver prototype.
For all three windings the width of tracks is 0.3 mm, the distance between the tracks is 0.16 mm, and the copper thickness 35 μm. An add-on SMD placement is possible as well. With this design of the PCB, a transformer with three galvanic isolated windings would have a thickness of only about 1.6 mm.

2.2 Limitations

With the spiral diameter $D$, the winding width $d$ (see Fig. 1), the inductance of a spiral winding (in one layer) is given by the following approximation:

$$ L = \frac{2.15 \text{ mH}}{\text{mm}} \frac{n^2 (D-d)}{1+2.72 \frac{d}{D-d}}. \quad (1) $$

Table 1 shows the calculated and measured inductances (Agilent 4294A with test fixture 16047E) of the primary and the secondary windings at 4 MHz without and with ferrite polymer composite (FPC) sheets. As can be seen eqn. (1) gives a good approximation also for multilayer spiral windings like $L_{pri}$ in Fig. 1.

<table>
<thead>
<tr>
<th>Tab. 1 Measured and calculated inductances</th>
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<tr>
<td>$L_{pri}$ (μH)</td>
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<tr>
<td>layers treated</td>
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<tr>
<td>calculated</td>
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<tr>
<td>measured $^{1)}$</td>
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<td>measured $^{2)}$</td>
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$^{1)}$ Without FPC sheets

$^{2)}$ With FPC sheets (Epcos FPC 351, thickness 200 μm)

From Table 1, the main disadvantage of PCB integrated transformers becomes obvious when compared, e.g., with toroidal core transformers. The attainable inductance in one layer is very small relating to the required PCB area. As a result a high switching frequency for the DC/DC converter is required.

Using the simple transformer model shown in Figure 3 and the impedance analyzer measurements for $R_i(f)$, $R_{sek}(f)$, $L_i(f)$, $L_{sek}(f)$ and $\sigma(f)$, the voltage transfer function $V/V_o$, the efficiency $\eta$ and the output power $P$ are calculated for two different load conditions $R$.

![Fig. 1](image1.png)

Layer structure of the PCB integrated transformer (developed prototype)

Considering electrical safety issues it is important to mention that the laminates in multilayer PCBs are typically made of two or more prepregs. In case of Fig. 1 the 360 μm laminate layers 1 and 3 are made of two prepregs with a nominal thickness of 200 μm [8]. A redundancy is realized this way since even in the case of an isolation failure (e.g. voids) in one laminate the second prepreg can withstand the isolation test voltage. With 360 μm thickness and 30 kV/mm minimum electrical field strength for the FR-4 prepregs in laminate layer 1, a value typical for materials like DURAVER-E-Cu 104i ML [8], 10.8 kV are calculated for the minimum breakdown voltage between copper layer one and two, which is enough for the required maximum blocking voltage of 1.2 kV. Between the primary and secondary side and between the two secondary sides a minimum creepage distance of approx. 2 mm is chosen respectively to reach a partial discharge value of more than 1.2 kV.

Moreover it is possible to hide the transformer inside the PCB by using more layers and embedded magnets [4]. With this technique [9] it is possible to use the area above the windings for other SMD components of the drive circuit.

![Fig. 2](image2.png)

Layer structure for an add-on PCB integrated transformer with only 1.2 mm thickness (example)

Figure 2 illustrates this advantage by showing the example of another embodiment where the transformer is placed as an add-on THT part on the backside of the driver PCB.
\( R_1(f) \): Frequency-dependent resistance of the primary winding \( L_1 \).
\( R_2(f) \): Frequency-dependent resistance of the secondary winding \( L_2 \).
\( L_1(f) \): Frequency-dependent inductance of the primary winding \( L_1 \).
\( L_2(f) \): Frequency-dependent inductance of the secondary winding \( L_2 \).
\( \sigma(f) \): Frequency-dependent leakage factor

**Figure 4** shows the voltage transfer function \( V/V_0 \), the efficiency \( \eta \) and the output power \( P \) for two different load conditions \( R \) as functions of the frequency \( f \).

\[
\begin{align*}
\eta &= V/V_0 \\
P &= P_W \\
R &= R_1 + R_2
\end{align*}
\]

With Fig. 4 the optimal operation frequency for the PCB integrated transformer can be chosen. It shows that the output power peaks at nearly 1 MHz (point A), while the efficiency peaks at a higher frequency. For a preferably high efficiency the switching frequency should be in the range of 4 MHz (point B). Above 4 MHz the voltage transfer function becomes highly dependent from the load. Therefore, as a trade-off between a high efficiency and an acceptable output voltage drop a switching frequency of 4 MHz (point C) is chosen for the DC/DC converter. This is a different approach compared to [10] where an additional capacitor at the secondary side reduces the transformer resonance frequency and induces a peak in the input impedance characteristic. Nevertheless, the winding resistance at this operation point is already relatively high due to skin and proximity effects.

Another disadvantage of PCB transformers is a high coupling capacity of about 20 pF between the primary and the secondary side of the driver. In addition electro-conductive areas nearby the windings must be shielded with FPC sheets as demonstrated for example in [4] and [11].

In spite of some limitations of PCB integrated transformers, which all can be handled in low power applications like gate drive power supplies, the advantage is to have a cost-efficient solution for very thin isolated multi winding transformers.

## 3 Operation Principle

### 3.1 Block Diagram

**Figure 5** displays the block diagram of the developed half-bridge driver. It shows the primary side power supply unit consisting of a 12 V powered single ended DC/DC converter, the PCB integrated transformer as described in Chapter 2, a control logic, and the resonant driven voltage clamped gate drive circuit comprising the MOSFETs T1-T4 with body diodes D1-D4 and the inductor \( L \).

It is assumed that the power switches in Fig. 5 have no internal gate resistances and can be characterized by an equivalent gate capacitance \( C_{eq} \).

**Fig. 5** Block diagram of the half-bridge driver

### 3.2 Resonance Driven Voltage Clamped Gate Driver Circuit

The following state analysis is related to the driver circuit in Fig. 5 and the state diagram shown in **Figure 6**.

**State 1:**
Transistor T1, T2 and T4 are switched off. To clamp the gate in the off-state the power switch T3 is switched on.

**State 2:**
When the control logic receives a turn-on signal, T1 is switched on for the pre-load time \( t_{PRE} \). During \( t_{PRE} \) the whole driving energy is stored in \( L \). At the end of state 2 T1 and T3 are switched off and the current through \( L \) commutates to D2.
State 3:
In state 3 the equivalent gate capacitance $C_{eq}$ is charged by transferring the energy stored in the resonance element $L$ to $C_{eq}$. This means that the gate voltage during the charge time $\Delta t_{ON}$ follows a sinusoidal waveform. When the stored energy in $L$ is exactly that for charging the gate, the peak value of the gate voltage is reached at the end of $\Delta t_{ON}$.

State 4:
To clamp the gate in the on-state $T4$ is switched on during State 4.

State 5:
When the control logic receives a turn-off signal, $T4$ is switched off and $T2$ is switched on with a small delay. $T2$ stays on for the discharge-time $\Delta t_{OFF}$. During $\Delta t_{OFF}$ the equivalent gate capacitance will be discharged by transferring the energy from the resonance element $C_{eq}$ to $L$.

State 6:
At the end of state 5 $T2$ is switched off and $T3$ is switched on. The current through $L$ commutates to $D1$. The energy in $L$ will be fed back during the reset time $t_{tRES}$ and stored in the DC link capacitor $C$ (see Fig. 5).

Fig. 6  State diagram

As Fig. 6 indicates, $T2$ could be used as a synchronous rectifier in state 3 and $T1$ could be used as a synchronous rectifier in state 6.

From the state diagram two principle limitations can be derived. These are:

$$T_{S_{\min}} = t_{PRE} + \Delta t_{ON} + \Delta t_{OFF} + t_{tRES}, \quad (2)$$

$$t_{OFF_{\min}} = t_{tRES} + t_{tPRE}, \quad (3)$$

$$t_{ON_{delay}} = t_{PRE}. \quad (4)$$

This means that the minimum switching period (2) is longer compared to conventional gate drive circuits due to the additional pre-charge state and reset state – but for the required maximum switching frequency it is still small enough. The limitation of the minimum turn-off time (3) is quite small as well. The little additional delay $\Delta t_{tRES}$ when turning on the power switch can easily compensated because it is a constant value.

4  Loss Analysis

When $T1$ and $T2$ are operated as synchronous rectifiers the losses in the gate drive stage as shown in Fig. 5 comprise conduction losses $(R_{DS}, R_L)$, switching losses in the full bridge, and the losses for driving the gates of the transistors $T1$-$T4$. Because of the comparatively low switching frequency $f_S$ in drive or high power DC/DC applications the switching losses and the gate drive losses in $T1$-$T4$ are assumed to be negligible.

With Fig. 5 and the state diagram Fig. 6 the following resistances are obvious for the different states:

$$R_{state2} = R_{DS,T1} + R_L + R_{DS,T3}, \quad (5a)$$

$$R_{state3} = R_{DS,T2} + R_L, \quad (5b)$$

$$R_{state5} = R_{DS,T2} + R_L, \quad (5c)$$

$$R_{state6} = R_{DS,T1} + R_L + R_{DS,T3}. \quad (5d)$$

The parameters have the following meanings:

$R_{DS,Tn}$  Drain-Source resistance of the MOSFETs ($T1$, $T2$, $T3$)

$R_L$  Series resistance of the inductor $L$

Since $R_L$ appears in each state (5a-5d) and is dominant it is assumed at this point that all conduction losses are lumped in a resistance $R_{AVG}$ with an average value given by:

$$R_{AVG} = \frac{R_{STATE2} + R_{STATE3} + R_{STATE3} + R_{STATE6}}{4}. \quad (6)$$

For arbitrary periodically waveforms the conduction losses in a resistance $R$ can be calculated:

$$P_R = R \sum_{i=0}^{T_S} I_L(t) \, dt. \quad (7)$$

With a linear approximation of the inductor current $I_L$ in the States 2 and 6 and the assumption that $I_L$ has a sinusoidal waveform in the States 3 and 5, the conductive losses in $R_{AVG}$ can be calculated using (5-7). The result is given by (8) and is valid when the damping of the resonant circuit is low. In addition, it is assumed that the waveform of the current $I_L$ is equal in State 2 and 6 and in State 3 and 5 respectively.

$$P_R = f_S \cdot R_{AVG} \cdot \frac{V_G^2}{L} \left( \frac{2}{3} \cdot \frac{f_S}{f_L} + \frac{\pi}{2} \cdot \frac{C_{eq} \cdot t_{tPRE}}{V_G} \right) \quad (8)$$

The reactive power necessary to charge the gate is:

$$P_c = C_{eq} \cdot V_G^2 \cdot f_S. \quad (9)$$
Since not all of this power can be recovered, the efficiency $\eta_{\text{RES}}$ of the resonant gate drive circuit is less than 1.

$$\eta_{\text{RES}} = \frac{P_c}{P_c + P_e}$$  \hfill (10)

With (8-10) it is obtained for the efficiency $\eta_{\text{RES}}$:

$$\eta_{\text{RES}} = \frac{1}{1 + \frac{R_{\text{avg}}}{\frac{2}{3}C_{\text{eq}}\Delta t_{\text{PRE}} + \frac{\pi}{2}\sqrt{L C_{\text{eq}}} \cdot \Delta t_{\text{PRE}}}}$$  \hfill (11)

5 Experimental Results

With a given equivalent gate capacitance $C_{\text{eq}}$, a given turn-on gate voltage $V_G$ for the power switch, and a given maximum turn-on delay time $t_{\text{ON-delay}}$ (4), there are two conditions for determining the inductor parameters $L$ and $I_{L,\text{max}}$.

$$L \geq C_{\text{eq}} \left( \frac{V_G^2}{I_{L,\text{max}}} \right),$$  \hfill (12)

$$L = \frac{t_{\text{ON-delay}} \cdot V_G}{I_{L,\text{max}}},$$  \hfill (13)

For the developed half bridge gate driver the following values were chosen: $V_G = 15$ V, $C_{\text{eq}} < 40$ nF, $t_{\text{ON-delay}} < 200$ ns (exact 180 ns), $L = 1 \mu$H, $I_{L,\text{max}} < 3$ A (exact 2.7 A).

For further measurements a 22 nF capacitor as an equivalent gate capacitance $C_{\text{eq}}$ is used. With an inductance of 1 $\mu$H, 180 ns for $t_{\text{PRE}}$ and a maximum current $I_{L,\text{max}}$ of 2.7 A, equation (12) shows that more energy is stored in $L$ than needed to charge the 22 nF capacitor, causing a preferred much faster turn-on time $\Delta t_{\text{ON}}$.

**Fig. 7** Measured gate drive signal with 22 nF equivalent gate capacitance

For measuring the losses of the gate drive stage both gate drive stages were disconnected from the power supply unit (see Fig. 5). In this configuration the voltage drop of the power supply unit while loaded with an ohmic resistor was measured. **Fig. 8** shows the voltages $V_{\text{BOT}}$ and $V_{\text{TOP}}$ with disconnected gate drive stages as functions of the output power, while loading $V_{\text{BOT}}$.

**Fig. 8** Secondary side power supply voltages $V_{\text{BOT}}$ and $V_{\text{TOP}}$ as functions of the output power, while loading $V_{\text{BOT}}$

From the datasheet (Fairchild FDC6327C) the following values for the drain-source resistances of the transistors T1, T2, T3 at 70°C junction temperature can be obtained:

$$R_{\text{DS,T1}} \approx 0.16 \Omega \quad \text{(PMOS)}$$

$$R_{\text{DS,T2}} = R_{\text{DS,T3}} \approx 0.08 \Omega \quad \text{(NMOS)}$$

Since the inductor $L$ is driven by a pulse current it is necessary to account the impedance at higher frequency with a Fourier analyses. With a linear approximated current $I_L$ (dotted line in Fig. 6) one obtains for $R_L$ a value of about 0.6 $\Omega$ (Epcs882462G4). With (5-6) the resistance $R_{\text{VG}}$ is about 0.8 $\Omega$. With that and (11) the efficiency $\eta_{\text{RES}}$ of the resonant gate drive circuit with synchronous rectifiers is calculated to 71%.
This means that the efficiency of the gate drive stage can be further improved when a synchronous rectifier is used, as proposed.

**Figure 9** shows a thermal image of the half-bridge driver when providing about 1.0 W equivalent gate driver power for the topside power switch.

The image shows only hotspots at the inductor $L$ and the MOSFETs T1, T2 with body diodes D1, D2 which are all in one tiny SuperSOT-6 package. The hotspots are only about 38 Kelvin above the ambient temperature. This slightly exceeds the defined requirement of 30 Kelvin.

### 6 Conclusion

With the novel concept of combining the advantages of a PCB integrated transformer and a resonance driven voltage clamped gate drive circuit an isolated half-bridge gate driver was developed. The gate driver has only 4.6 mm thickness and is able to deliver one watt equivalent gate drive power for the top or bottom power switch with only 38 Kelvin temperature rise at the hotspots. A comparison of the measured efficiency of the gate drive stage without a synchronous rectifier mode and the calculated efficiency with a synchronous rectifier for T1 and T2, as proposed in Chapter 3, shows that the efficiency could further improved - what has to be proved by further experiments.

### 7 Literature


