Abstract—The SiC MOSFETs are finding their niche in 1 kV range, which is currently dominated by Si IGBTs. Thus, the frequencies of power converters could be increased remarkably and the power density could be higher. The gate driver for SiC MOSFET would affect the performance significantly, and a direct transplant of gate driver for Si MOSFET would not be reliable and efficient. This paper attempts to evaluate the design of gate driver for SiC MOSFETs. On the basis of studying the characteristics of SiC MOSFET, new requirements of gate driver for SiC MOSFETs are derived. A magnetic isolated gate driver is fabricated and experimental results based on an open loop BUCK circuit are presented. In order to optimize the performance of SiC MOSFETs, the gate drive loop must be carefully designed.

Keywords—SiC MOSFET; isolated gate driver; high frequency;

I. INTRODUCTION

With the continuous development of power converters for a range of applications, the demand for higher power density and higher efficiency increased significantly. To design converters with ever increasing power densities, the converters should be operated at higher switching frequencies and/or higher temperatures. At higher frequencies the volume of the magnetic components reduces, however, the switching losses of the semiconductor devices decrease with the increase of switching frequency. For high frequency operation above 100 kHz, the silicon (Si) MOSFET has been the device of choice but they are limited in voltage rating (above 600V) and operating temperature range [1] [2]. For higher voltage and temperature applications, Si IGBTs offer low conduction loss but the switching frequency is limited due to turn-off current tail [3]. Research indicates that power electronic devices constructed from silicon carbide (SiC) have great potential [4] [5] [6]. The SiC power semiconductors are characterized by outstanding performance concerning their voltage blocking capability, on-state voltage drop, switching speed, and thermal resistance. Accordingly, SiC devices should allow the realization of highly compact converter systems with lower switching and conduction losses.

Silicon carbide device technology has gone from research to commercial production over the past decades. After the world’s first commercial SiC power diodes were made available to the private sector in 2001 by Infineon, commercial SiC power devices developed rapidly. In 2011, the most concerned commercial SiC MOSFET was first released by CREE [7]. Although SiC MOSFET is a superior switch compared to its silicon counter-parts, there are some differences in characteristics when compared to what is usually expected with high voltage silicon MOSFET. SiC MOSFET is expected to be operated at high frequency with lower losses, while the switching and conduction losses are closely related to the performance of gate driver. In order to realize the full potentials of the SiC MOSFETs, a direct drop-in replacement in existing applications is inappropriate, and it’s necessary to design a simple and reliable gate driver for SiC MOSFETs.

This paper aims at evaluating the design of isolated gate driver for SiC MOSFET. The characteristics of SiC MOSFET are introduced and the requirements for driving the SiC MOSFETs are analyzed in Section II. A magnetic isolated gate driver is described and some design details are discussed in Section III. Then Section IV presents the experimental results and a brief conclusion is given in Section V.

II. CHARACTERISTICS AND DRIVING REQUIREMENTS OF SiC MOSFETs

The SiC MOSFET has unique capabilities that make it a superior switch when compared to its silicon counterparts. The advantages of high operating temperature, high voltage capability with low switching losses have been documented extensively in the literature. (Owing to its superior switching performance, the SiC MOSFET is a preferred choice for high voltage and high power density applications.) However, there are some unique operating characteristics that need to be understood so that the device can be used to its full potential. This is especially true in the procedure of designing an appropriate gate driver for SiC MOSFETs.

The output characteristics of a typical 1.2kV 20A SiC MOSFET (CMF10120D from CREE) and a typical 1kV 21A Si MOSFET (IXTK21N100 from IXYS) are shown in Fig 1 and Fig 2 respectively. The curves of the two MOSFETs are different. The transition from triode (ohmic) to saturation (constant current) regions of SiC MOSFET spreads over a wider range of drain current and there is also a reduction of output impedance adding to the slope of the drain current in the saturation region. This is caused by the modest transconductance and short channel structure of the device. These effects need to be considered carefully when using the device. For gate driver, the low transconductance illustrates the need for a large amount of gate drive voltage. In order to get a lower on-resistance, a higher gate drive voltage swing is needed than what is customary with Si MOSFET. The rate of rise of
gate voltage will have a greater effect on the rate of rise of the drain current. Therefore, the gate drive needs to supply a fast rise and fall time gate pulse to maximize switching speed. Presently, +20V gate drive is recommended [3]. Besides, the SiC MOSFET has a relatively lower threshold voltage compared to common Si MOSFET, especially at high temperature. Thus, negative gate bias should be considered.

The modest transconductance and the low threshold voltage of SiC MOSFET also make the device more sensitive to gate voltage anomalies. Therefore, the fidelity of the gate signal must be carefully controlled to minimize the possibility of unintentional device turn-on or turn-off. To achieve fast switching time, the gate drive interconnections need to have minimum parasitics, especially stray inductance. This requires the gate driver to be located as close as possible to the SiC MOSFET. Care should be taken to minimize or eliminate ringing in the gate drive circuit. This can be achieved by selecting an appropriate external gate resistor. Negative gate bias is helpful to mitigate the effects of low threshold voltage. It is also important to minimize the effects of drain current coupling into the gate drive from common source inductance. Therefore, a Kelvin connection for the gate drive is recommended, especially if the gate driver cannot be located close to the SiC MOSFET. Ferrite beads (nickel-zinc recommended) in lieu of or in addition to an external gate resistor are helpful to minimize ringing while maintaining fast switching time.

A plot of gate voltage versus gate charge for the SiC MOSFET is shown in Fig 3. The Miller plateau is not as flat as observed in typical Si MOSFETs. The comparison results show that the SiC MOSFET has noticeably lower gate charge, albeit without the very flat plateau region. The significantly lower gate charge of the SiC MOSFET tends to offset the higher gate drive voltage requirement. The product of gate charge and gate voltage of SiC MOSFET is comparable to or lower than other devices. Therefore, the higher voltage swing does not adversely affect gate drive power requirements.

As with any majority carrier device, the SiC MOSFET has no turn-off current tail. So the amount of drain voltage overshoot and parasitic ringing is noticeably higher. The higher ringing is of concern because of the SiC MOSFET’s lower transconductance and low threshold voltage reduces gate noise immunity. The high level of drain current di/dt can couple back to the gate circuit through any common gate/source inductance. The most direct way to control this is by minimizing or eliminating parasitic inductance and by carefully choosing the value of external gate resistance. The turn-off gate noise immunity can be also improved by using a negative gate bias.

III. ANALYSIS OF MAGNETIC ISOLATED GATE DRIVER FOR SiC MOSFETs

The gate drive circuits for MOSFETs can be divided into two groups: isolated gate drivers and non-isolated gate drivers. Since the blocking voltage of SiC MOSFET is higher than 1kV, isolated gate driver should be necessary to meet the isolation requirement. Either optical or magnetic is a common way for providing isolation. For gate drive design, both optical and magnetic can transfer the signal and power from the signal IC to the power device. An optical isolated gate driver suitable for testing and evaluating SiC MOSFETs in a variety of applications was described in CREE’s technical documentations [7]. In this paper, a magnetic isolated gate driver is investigated and tested.

As shown in Fig 4, a simple typical magnetic isolated gate driver is adopted. Since the output of the UC3845 is only ±500mA, a totem-pole circuit is added to improve the driving
current capability. The NPN transistor used in the totem-pole is KSD882 and the PNP transistor is KSB772. The dc collector current of the transistors is 3A and the pulse current could be 7A, which would be large enough to drive MOSFET. The transformer is unidirectional magnetized and reset by the blocking capacitor. In the steady state, the blocking capacitor has a constant dc voltage and varies with the duty cycle of the PWM signal. Therefore, the second side voltage of the transformer also varies with the duty cycle, which may disable the gate driver. In order to offset the effects of the blocking capacitor, another capacitor should be added to the second side of the transformer. Then the gate voltage would hardly vary with the duty cycle. The two zener diodes in reverse series connection clamp the amplitude of the positive and the negative gate pulse voltage respectively. It can meet the requirements of wide voltage swing and negative voltage bias for driving SiC MOSFET. All the circuit should be put as close as possible to the SiC MOSFET.

The gate drive circuit can be simplified to an equivalent circuit shown in Fig 5. \( U_{d_{gs}} \) is the equivalent gate drive voltage of the second winding and the blocking capacitor, \( L_r \) is the equivalent inductance of the leakage inductance of the transformer and the stray inductance in the drive circuit, \( R \) is the gate drive resistance and \( C_{gs} \) is the gate-source capacitance. This loop is a typical second order circuit. As we all known, there is a critical damping state when the resistance was chosen using equation (1).

\[
R = 2 \sqrt{\frac{I_r}{C_{gs}}} \tag{1}
\]

If \( R \) is higher, the circuit would be over damping, and the switching speed would be slower. For high switching frequency driver, \( R \) is relatively lower. Then ringing would appear on the \( C_{gs} \). Compared to Si MOSFET, the \( C_{gs} \) of SiC MOSFET is lower. Therefore, SiC MOSFET is more sensitive to the ringing. Even worse, referenced to the datasheet of CREE’s SiC MOSFET [7], the gate-source voltage window is -5V to +25V. In order to fully exploit the advantage of SiC MOSFETs, the recommended drive voltage should be +20V/-2V. However, the gate-source voltage window of Si MOSFET could usually be -25V to +25V, and the drive voltage signal is only +15V/0V. That’s to say: the gate drive voltage ringing could invalidate SiC MOSFET easier.

Since we want to gain both fast switching speed and low ringing, the \( L_r \) must be minimized to reduce the gate drive resistance. First, the pulse transformer should be winded with a low leakage inductance winding method, such as "the sandwich" winding method. The windings should also be uniformly distributed. Then the stray inductance of the PCB board needs to be carefully considered. The gate driver must be put as close as possible to the SiC MOSFETs. For example, the output signal of the driver should be connected to the gate and source within the minimum loop length.

**IV. EXPERIMENTAL RESULTS AND DISCUSSION**

As mentioned in the earlier section, the high switching frequency is crucial to achieve high power density converter. Therefore, the mentioned gate drive circuit for SiC MOSFET operates at frequencies beyond 100 kHz and the corresponding results are presented in this section. The circuit used to test the gate driver is an open loop BUCK circuit as shown in Fig 6. The load is resistive but it has considerable amount of stray inductance.

Fig 7 shows the switching waveforms at 100 kHz for 300 V input dc voltage under open loop operation. The load resistance is 30 Ohm and the open loop duty cycle is fixed at 0.4, which corresponds to 4 A of current in the load. Under this condition, the BUCK is working in continuous current mode. The turn-on and turn-off transitions of the gate-source voltage waveform are not very smooth because of the Miller effect. The top and bottom of the waveform are not flat due to the charge and discharge of the capacitor \( C_{dc_s} \) in Fig. 4.

As discussed in earlier sections, a higher gate drive voltage swing is needed for SiC MOSFETs to get a lower on-resistance. In the test, the gate drive voltage was varied from +12V to +20V with the same gate resistance, and the corresponding
efficiencies were compared. However, there is not a significant difference due to the great lower on-resistance of SiC MOSFETs and the relatively low load current. The conduction power losses are not big deal compared to the 480W output power. That's to say, higher gate drive voltage for SiC MOSFETs is not a matter of great concern in low current applications.

The gate resistance varied with a fixed gate drive voltage of +18V. The corresponding efficiencies are shown in Fig 8. The efficiency is relatively lower than the common BUCK circuit, that's because of the high gate resistance. The SiC MOSFET is more sensitive to the ringing and the minimum allowable negative voltage is only -5V, what's worse is that negative gate bias should be considered. Since the gate driver board is a preliminary one, and is not well designed enough to minimize the leakage inductance, a relative higher gate resistance is applied to avoid the failure of the SiC MOSFETs. From Fig 8, it is clear that when decreasing the gate resistance, even higher efficiency could be reached. That means the switching speed has a great impact on the switching losses of SiC MOSFETs, and the gate resistance play a key role in the switching process.

At higher switching frequency, the switching losses become more crucial to the overall efficiency. Fig 9 shows device switching waveform for 300V at 400 kHz switching frequency. Compared to Fig.7, it can be seen that there is significant amount of LC oscillation at switching transient of gate-source voltage and the SiC MOSFET is much easier to fail. This is due to resonance in the gate drive circuit. With the same gate resistance of 39 Ohm, the measured efficiency decreased almost 4 percentage points when the frequency was increased from 100 kHz to 400 kHz. The switching losses of SiC MOSFETs tremendously degrade the performance of the converter, not only the efficiency. The horrible heat generated by the losses would also be a heavy burden for the converter.

As a conclusion, careful design of the gate drive loop to permit a minimum gate resistance would greatly optimize the performance of the SiC MOSFETs. Then higher frequency operation of SiC MOSFETs could be possible.

V. CONCLUSION

This paper attempts to evaluate the design of high frequency magnetic isolated gate driver for SiC MOSFETs. The main characteristics of SiC MOSFET that affect the design of gate driver are introduced. And the corresponding requirements for SiC MOSFET gate driver are given. A magnetic isolated gate drive circuits for SiC MOSFET is analysed. Some details in the design proceeding are also pointed out. The experimental test of an open loop BUCK circuit is provided for verification purposes. The gate driver is operated at frequencies beyond 100 kHz. In conclusion, high frequency converters based on SiC MOSFETs could be realized only when the gate drive loop was well designed to permit a minimum gate resistance.

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