Secondary-Side Phase-Shift-Controlled ZVS DC/DC Converter With Wide Voltage Gain for High Input Voltage Applications

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Abstract—In this paper, a soft-switching dc/dc converter with secondary-side phase-shift control strategy is proposed to improve the conversion efficiency and minimize the primary switch voltage stress in the high input voltage applications. Zero-voltage-switching performance is achieved for both the primary- and secondary-side power devices in a wide load range to reduce the switching losses due to the secondary-side phase-shift control scheme. Furthermore, compared with the conventional phase-shift control mechanism, the circulating current at the freewheeling stage is effectively suppressed as well to minimize the conduction losses. Moreover, the voltage stress of the primary switches is only half of the input voltage by employing the improved three-level structure, which makes the low-voltage rated power devices available to improve the circuit performance. In addition, the converter can work in the buck, balance, and boost modes to achieve a relatively wide input voltage range, which is an expected advantage for the communication power system to minimize the electrolytic capacitor with an acceptable hold-up time. The operation principle is analyzed and experimental results of a 1-kW 100-kHz prototype are provided to verify the effectiveness and the advantages of the proposed converter.

Index Terms—High input voltage applications, secondary-side phase-shift control, wide voltage conversion range, zero-voltage switching (ZVS).

I. INTRODUCTION

In the high input voltage applications, the high-voltage rated switching devices are commonly required to construct the conventional full-bridge dc/dc converters. However, the conduction resistor $R_{DS_{ON}}$ of the switching devices increases exponentially as the voltage stress rises, which results in the severe conduction losses. Recently, many research contributions have been carried out to make the low-voltage rated power devices available in the high input voltage conversion systems. One of the main concepts is to connect the switches in series to sustain the high voltage stress. In [1], three pairs of series switches are connected in the primary side, which reduces the switch voltage stress to only one-third of the high input voltage. This topology is further extended to $N$ pairs of series switches [2], where the switch voltage stress is reduced to one $N$th of the high input voltage. Unfortunately, the number of the transformer windings as well as the control complexity increases as $N$ goes up. A rectifier is added to the middle pair of the three series switch pairs to realize the voltage autobalance of the series input capacitors [3]. Nevertheless, the auxiliary snubber and the extra rectifier increase the power losses. Apart from the bridge-type topology, Qian and Lehman [4] present a coupled dual-interleaved flyback converter. The voltage stress is reduced to half of that of the conventional flyback converter. However, it still remains higher than half of the input voltage due to the inversely addressed output voltage in the primary side of the transformer. A three-switch active-clamped forward converter is introduced in [5], whereas the voltage stress is only reduced to around the input voltage and the soft-switching is not achieved, which impacts the efficiency improvements.

Although the conventional phase-shift full-bridge (PSFB) converter has some clear advantages in the low-voltage applications, the circulating current at the freewheeling stage causes additional losses, especially when the duty cycle is small. Large amount of work has been done to solve this problem. Generally, some extra components are added to suppress the circulating current to reduce power losses. For instance, an auxiliary transformer or an extra winding is introduced to the converter, through which the energy in the inductor is fed back to the input or output terminals [6]–[8]. In [9] and [10], the main transformer has a center tap on the secondary winding, and a capacitor and some auxiliary diodes are connected in the secondary side to suppress the circulating current and recycle the energy of the inductor. A blocking capacitor and a saturable inductor instead of an usual inductor are adopted in the primary side to eliminate the freewheeling current and achieve zero-current switching (ZCS) of the lagging leg with extended load range [11], [12], but the saturable inductor causes additional core losses due to the large peak-to-peak flux density, which may result in the high inductor temperature. Furthermore, the secondary-side diodes in the conventional PSFB converters are connected in series with the active switches to reduce the circulating current and minimize...
the leakage inductance [13]–[15]. Unfortunately, the two active secondary-side switches cause extra losses especially in the high step-down applications. All the aforementioned improved converters are derived from the conventional PSFB topology by inserting some additional power components. These converters have to sacrifice the inherent structural simplicity of the PSFB converters to tackle the problem of the circulating current and voltage spikes on the secondary rectifier diodes. Unfortunately, other unexpected problems emerge, such as the complex circuit structure, low controllability, and extra power losses.

In addition, in order to reduce the primary switch voltage stress, the conventional three-level structure is widely adopted and discussed in [16]–[18], and the switch voltage stress is reduced to half of the input voltage, which is essential for the high input voltage applications. However, the circulating losses and the voltage spikes on the secondary-side diodes still exist with the conventional phase-shift control scheme.

In order to overcome the disadvantages of the conventional phase-shift control scheme, secondary-side phase-shift (SSPS) control strategy is proposed in [19], [20], where the duty cycle of both the primary and secondary active switches keeps 0.5 and the phase-shift angle between the primary and secondary switches is employed as the control freedom to regulate the output voltage. With the SSPS control strategy, the output filter inductor in the conventional phase-shift converter can be removed to simplify the circuit structure. Moreover, the freewheeling current is effectively suppressed and the voltage spikes on the secondary-side switches are eliminated. However, how to employ the advanced secondary-side phase-shift control strategy in the high input voltage applications with reduced primary switch voltage stress still remains unclear and it is necessary to carry out more scientific discovery and research exploration. Besides, how to achieve high-efficiency dc/dc conversion in a wide voltage range is an emergent research topic in the renewable energy applications and communication power systems [21], [22]. For example, the output voltage of the photovoltaic (PV) array may fluctuate by over 100% due to the change of the ambient environment. The adopted front-end dc/dc converters in the grid-connected PV system have to provide high-efficiency conversion with a wide voltage conversion range. Also in the communication power supply system, the front-end dc/dc converters with a wide voltage conversion range are required to extend the hold-up time with minimum electrolytic capacitors, which cannot only improve the power density, but also enhance the system reliability. As a result, how to achieve high-efficiency and wide voltage gain conversion with the advanced secondary-side phase-shift control strategy is another interesting and valuable innovation.

An SSPS-controlled ZVS dc/dc converter with reduced switch voltage stress is proposed in this paper. The improved three-level structure is employed in the primary side to reduce the switch voltage stress to half of the input voltage. As a result, the low-voltage rated devices can be used to improve the circuit performance. In addition, due to the SSPS control scheme, ZVS switching is achieved for all the power devices in a wide load range without any auxiliary components. Different from the conventional primary-side phase-shift converters, there is no circulating current at the freewheeling stage, which reduces the conduction losses effectively. And the overshoots on the rectifier are effectively suppressed since the rectifier is clamped to the output voltage. Moreover, the converter can work in three modes, including the buck, balance, and boost modes, which means the converter has a wide voltage conversion range. All the advantages make the proposed converter competitive in the high input voltage and wide range conversion applications, such as the three-phase front-end communication power systems.

II. PROPOSED CONVERTER AND OPERATIONAL PRINCIPLE

The proposed SSPS-controlled ZVS dc/dc converter for the high input voltage application is shown in Fig. 1, where all of the four primary switches have the constant duty cycle of 0.5. The outer pair of switches $S_{p1}$ and $S_{p4}$ turns ON and OFF simultaneously, while the inner pair of switches $S_{p2}$ and $S_{p3}$ shares the same gate signal. The two pairs of the primary switches operate in the complementary manner. The two secondary-side switches $S_{s1}$ and $S_{s2}$ also act with 0.5 duty cycle complementarily. The phase-shift angle between the primary and secondary active switches is employed to control the output voltage and power. $L_{Lk}$ stands for the transformer leakage inductance, which usually includes an external inductor if the practical leakage inductance is not large enough to realize the expected circuit operation. The input series capacitors $C_1$ and $C_2$ have the same capacitance to clamp the primary switch voltage stress to half of the input voltage. $r_p$ and $v_s$ are the voltages on the primary side and the secondary side of the transformer, respectively. And $i_p$ and $i_s$ are the primary and secondary currents through the transformer with the positive direction shown in Fig. 1.

The operations of the proposed converter are elaborated in this section. According to the work conditions of the primary current, the converter has three different operation modes, namely continuous current mode 1 (CCM1), continuous current mode 2 (CCM2), and discontinuous current mode (DCM), respectively. Considering only half of the input voltage is imposed on the primary side of the transformer, in order to simplify the analysis, the gain $G$ is defined as

$$G = \frac{2NV_{out}}{V_{in}} \quad (1)$$

where $V_{in}$, $V_{out}$, and $N$ are the input voltage, output voltage, and transformer turns ratio $n_1/n_2$, respectively. The converter can work in the buck mode ($G < 1$), balance mode ($G = 1$), and boost mode ($G > 1$). And the primary current increases,
keeps constant, and decreases at the power-transferring stage of the three modes, respectively.

A. CCM1 Mode

The key voltage and current waveforms in the balance mode are shown in Fig. 2. The corresponding equivalent circuit at every stage is illustrated in Fig. 3. As given in Fig. 2, $\phi$ is the phase-shift angle between the leading primary switches and the corresponding lagging secondary active switch. $\beta$ is the time interval during which the primary current returns to zero after the primary active switches turn OFF. $\phi \geq \beta$ is met in the CCM1 mode. Due to the symmetrical operations, only the first seven stages are analyzed as follows.

Stage 1 [$\theta_0, \theta_1$]: During this interval, the primary current $i_p$ flows reversely through $S_{p1}$ and $S_{p4}$. The power is delivered from $L_{LLk}$ to the input and the secondary side. The output voltage $V_{out}$ is adversely addressed in the secondary side of the transformer. Due to the negative voltage across the leakage inductor, the current $i_p$ declines rapidly, which is expressed as

$$i_p = i_p(\theta_0) + \frac{NV_{out}}{L_{LLk}}(1/G + 1)(\theta - \theta_0), \quad (\theta_0 \leq t < \theta_1).$$

In the CCM1 mode, Stage 1 lasts for phase angle $\beta$. That is

$$\beta = \theta_1 - \theta_0.$$  (3)

Stage 2 [$\theta_1, \theta_2$]: At $\theta_1$, $i_p$ reaches zero and starts increasing linearly due to half of the input voltage across the leakage inductor. As $i_p$ reverses, the secondary-side current $i_s$ begins to circulate freely through $S_{s1}$ and the antiparallel diode of $S_{s2}$. The voltage of both sides of the transformer is zero. The power is delivered from $V_{in}$ to $L_{LLk}$. $i_p$ is regulated by

$$i_p = i_p(\theta_1) + \frac{NV_{out}}{GL_{LLk}}(\theta - \theta_1), \quad (\theta_1 < \theta \leq \theta_2).$$  (4)
In the CCM1 mode, \( i_p \) keeps increasing at this stage. As a result, the ZVS-on of \( S_{s2} \) is achieved naturally. There is not any extra condition to be satisfied for the ZVS-on operation of the secondary-side switches.

**Stage 3 \([\theta_2, \theta_3] \):** \( S_{s1} \) turns OFF at \( \theta_2 \) and \( C_{s1} \) is charged to \( V_{\text{out}} \) by \( i_s \) at the end of this stage. \( i_p \) is regulated by (4) until \( \theta_3 \). And the phase angle \( \varphi \) is expressed as

\[
\varphi = \theta_3 - \theta_0.
\]

\((5)\)

**Stage 4 \([\theta_3, \theta_4] \):** When \( C_{s1} \) is charged to \( V_{\text{out}} \) at \( \theta_3 \), \( D_{s1} \) becomes forward-biased. \( i_s \) flows through \( D_{s1} \) and the body diode of \( S_{s2} \), delivering the power from \( V_{\text{in}} \) to the load. Most of the power is transferred to the load during this stage which is named as the power-transferring stage. The primary current can be obtained as

\[
i_p = i_p(\theta_3) + \frac{NV_{\text{out}}}{L_{Lk}} \left(1/G - 1\right)(\theta - \theta_3), \quad (\theta_3 < \theta < \theta_7).
\]

\((6)\)

In the balance mode, \( G = 1 \) and \( i_p \) keeps constant during this stage, as shown in Fig. 2. If the converter operates in the buck or boost modes, \( i_s \) will increase or decrease, respectively, during this stage.

**Stage 5 \([\theta_4, \theta_5] \):** At the beginning of this interval, \( S_{s2} \) turns ON with ZVS and begins working in the synchronous rectification mode. The primary current is also regulated by \((6)\).

**Stage 6 \([\theta_5, \theta_6] \):** At \( \theta_5 \), \( S_{p1} \) and \( S_{p4} \) turn OFF. ZVS turn-off soft switching performance for \( S_{p1} \) and \( S_{p4} \) is achieved due to the parallel capacitors \( C_{p1} \) and \( C_{p4} \). \( C_{p1} \) and \( C_{p4} \) are charged, while \( C_{p2} \) and \( C_{p3} \) are discharged by the primary current. All the parallel capacitors can be charged or discharged completely before \( S_{p1} \) and \( S_{p2} \) turn ON only if the energy stored in \( L_{Lk} \) is large enough. The ZVS condition will be analyzed further in the next section.

**Stage 7 \([\theta_6, \theta_7] \):** When \( C_{p2} \) and \( C_{p3} \) are discharged completely, the antiparallel diodes of \( S_{p2} \) and \( S_{p3} \) are forward-biased, which enables ZVS-on of \( S_{p2} \) and \( S_{p3} \). The primary current decreases rapidly due to the negative voltage across \( L_{Lk} \), which is the sum of \( \frac{1}{2}V_{\text{in}} \) and \( NV_{\text{out}} \). At the end of Stage 7, \( i_p \) becomes negative but has the same absolute value as that at the beginning of Stage 1, which is expressed as

\[
i_p(\theta_7) = -i_p(\theta_0).
\]

\((7)\)

The succeeding operation stages from 8 to 13 are similar to Stage 1–7.

**B. CCM2 Mode**

The above analysis of the CCM1 mode is based on the condition of \( \varphi \geq \beta \), which means the secondary-side semiconductor devices commutate after \( i_p \) returns to zero. If that is not the case, i.e., \( \varphi < \beta \), the circuit will enter the CCM2 mode. The key waveforms of the CCM2 mode are shown in Fig. 4 and the operational stages are illustrated in Fig. 3. As shown in Fig. 4, in the CCM2 mode, the converter can only work in the buck mode because the voltage across the leakage inductor must be positive in order to increase the primary current during the power-transferring stage. Otherwise, there would be almost no current through the inductor and the power cannot be delivered to the load.

There are also 14 operational stages in a switching period of CCM2. The power-transferring stage and the primary MOSFETs switching stages are similar to the CCM1 mode, while the main differences between CCM1 and CCM2 can be observed in the secondary-side MOSFETs switching intervals.
As a result, the Stages 2–5 are analyzed in detail with the description of the other stages omitted.

Stage 2 \([\theta_1, \theta_2]\): Before \(i_s\) returns to zero, \(S_{s1}\) turns OFF. The operation of the converter does not change, except that the current through \(S_{s1}\) changes to flow through the body diode. \(i_p\) is still regulated by (2), while the phase-shift angle is expressed as

\[
\varphi = \theta_2 - \theta_0.
\]

Stage 3 \([\theta_2, \theta_3]\): Before \(i_p\) declines to zero, there is no current through the body diode of \(S_{s2}\), and the voltage of \(S_{s2}\) still equals the output voltage \(V_{out}\). As a result, \(S_{s2}\) turns ON with hard switching. Therefore, ZVS is lost for the secondary-side switches in CCM2. After turning ON of \(S_{s2}\), the current through \(D_{s2}\) is shunted through \(S_{s2}\). The secondary-side current circulates through \(S_{s1}\) and \(S_{s2}\) freely, and the secondary winding of the transformer is shorted. Therefore, the output voltage is decoupled from the transformer, and the load is supplied by only the output capacitor.

The primary current at this stage is also regulated by (4). With only half of the input voltage across the leakage inductor, the current falling rate is smaller compared to CCM1 and it takes longer time for \(i_p\) to decline to zero. In addition, the power of the leakage inductor only returns to the input. As a result, less power is transferred to the load than CCM1 mode during the intervals prior to the power-transferring stage.

Stage 4 \([\theta_3, \theta_4]\): As the primary current reverses, the parallel capacitor of \(S_{s1}\) is charged by the secondary-side current. And

\[
\beta = \theta_4 - \theta_0.
\]

Stage 5 \([\theta_4, \theta_5]\): Most of the power is transferred during this stage with \(i_p\) regulated by (6). This stage is the same as Stage 5 of CCM1 except that \(i_p\) is zero at the beginning of this stage. That is, \(i_p(\theta_4) = 0\). As to the CCM1 mode, \(i_p\) is larger than zero at the beginning of the power-transferring stage. Assuming \(G\) and \(V_{out}\) are the same for both the modes, it is clear that less power is transferred to the output terminal in CCM2 than in CCM1 during the power-transferring stage. In addition, as explained in Stage 3 of CCM2 mode, the converter transfers less power before the power-transferring stage. As a whole, less power is transferred in the CCM2 mode than the CCM1 mode during a whole switching period, which will be illustrated further in the next section.

When the converter works in the boost or balance modes, i.e., \(G \geq 1\), \(i_p\) keeps zero at the power-transferring stage and no power is transferred to the load. Thus, the converter has to work in the buck mode if it enters the CCM2 mode.

However, the CCM2 mode is not recommended for the practical applications. The secondary active switch turns ON before the primary current returns to zero. As a result, ZVS-on is lost for the secondary-side switches. And it costs longer time than CCM1 mode for the primary current to return to zero since the inductor voltage is only half of \(V_{in}\). This results in extra power losses due to the secondary-side circulating current through \(S_{s1}\) and \(S_{s2}\).

C. DCM Mode

When the converter works in the boost mode, the primary current may decline to zero at the power-transferring stage if the load is relatively light. This is the DCM mode and the operation waveforms are displayed in Fig. 5. Since the operations of DCM are similar to the CCM1 and CCM2 modes, the operation analysis of DCM is not provided. The primary current \(i_p\) at Stage 1 \([\theta_0, \theta_1]\) and Stage 2 \([\theta_1, \theta_2]\) are also regulated by (4) and (6), respectively.

Since \(S_{s1}\) has turned ON before \(i_s\) starts to flow through it at \(\theta_0\) in DCM, ZCS is achieved for \(S_{s1}\) naturally. No extra condition has to be satisfied for ZVS-on of the secondary-side switches.

Different from CCM1 and CCM2, \(i_p\) has returned to zero before the primary switches commutate at \(\theta_0\), which means \(\beta = 0\) and \(\varphi \geq \beta\) is always satisfied. As a result, the secondary side is not powered by \(L_{Lk}\) after the primary switches transition at Stage 3 and all of the power is transferred through the transformer only at Stage 2.

As shown in Fig. 5, \(i_p\) must keep decreasing linearly to zero at Stage 2. Therefore, the converter can only work in the boost mode for DCM and \(G \geq 1\), which means the converter cannot switch directly between DCM and CCM2 where \(G \leq 1\).
III. Converter Performance Analysis

A. Output Characteristics

1) CCM1 Mode: According to the analysis of the CCM1 mode in the previous section, the average primary current can be obtained as

$$I_{av} = \frac{i_p(\theta_0)}{2\pi} + \frac{i_p(\varphi) \cdot (\varphi - \beta)}{2\pi} + \frac{[i_p(\varphi) + i_p(\pi)] \cdot (\pi - \varphi)}{2\pi}.$$  

(10)

And the transferred power is expressed as

$$P_{out} = \frac{1}{2}V_{in}I_{av}. \quad (11)$$

For simplification, the phase-shift angle $\varphi$ is normalized as $D = \varphi/\pi$ and the base power $P_b$ is normalized with the base power $V_{out}$.

$$P_b = \frac{(NV_{out})^2}{2\pi f_s I_{LL}}, \quad (f_s = \text{switching frequency}). \quad (13)$$

From (1)–(7), (10), and (11), the output power can be obtained as

$$P_{CCM1}(G, D) = \pi P_b \left[1 + G - 2G^2 + 4D(1 + G + G^2) - 2D^2(1 + 2G + G^2)\right] / 2G(2 + G)^2.$$  

(14)

2) CCM2 Mode: If $\varphi$ is smaller than $\beta$, the operation enters the CCM2 mode. According to the analysis of the CCM2 mode in the previous section, the gain $G$ should be smaller than 1. The average primary current can be expressed as

$$I_{av} = \frac{[i_p(\theta_0)] + i_p(\varphi)] \cdot \varphi + \frac{i_p(\varphi) \cdot (\beta - \varphi)}{2\pi} + \frac{i_p(\pi) \cdot (\pi - \beta)}{2\pi}.$$  

(15)

From (2), (4), (6)–(9), and (15), the output power can be obtained as

$$P_{CCM2}(G, D) = \pi P_b \left[(1 + 4G)(1 - G) + 2(-2 + 2G - G^2)G^2\right] / 2G(2 - G)^2, \quad (G < 1).$$  

(16)

At the boundary between the CCM1 and CCM2 modes, $\varphi = \beta$. Applying the volt–second balance principle to the leakage inductor, the boundary condition can be obtained as

$$\varphi_{b1} = (1 - G)\pi / 2.$$  

(17)

For a given $G$ smaller than 1, if $\varphi$ becomes smaller than $\varphi_{b1}$, $\varphi$ would always be smaller than $\beta$, and the converter works in the CCM2 mode; otherwise, $\varphi$ is always larger than $\beta$, and the converter enters the CCM1 mode.

3) DCM Mode: When $i_p$ becomes discontinuous, the converter goes into the DCM mode. As analyzed in the previous section, the gain $G$ should be larger than 1. And the average primary current can be obtained as

$$I_{av} = \frac{i_p(\varphi) \cdot (\varphi + \gamma)}{2\pi}.$$  

(18)

From (10), (11), and (18), the output power can be expressed as

$$P_{DCM}(G, D) = \pi D^2 P_b / 2G(G - 1)^2, \quad (G > 1).$$  

(19)

As analyzed in the previous section, the converter can only work in the boost mode for DCM and $G > 1$, which means the converter cannot switch directly between DCM and CCM2 where $G < 1$. The boundary between the DCM and CCM1 modes is governed by

$$\varphi_{b2} = \frac{G - 1}{G}\pi.$$  

(20)

For a given $G$ larger than 1, if $\varphi$ becomes smaller than $\varphi_{b2}$, the primary current would be discontinuous and the converter would enter the DCM mode; otherwise, the converter will work in the CCM1 mode.

In summary, the relationship between the gain $G$ and the operation modes is illustrated in Table I. The converter can work in the buck, balance, or boost modes in the CCM1 mode. And the gain can only be below and over 1 in CCM2 and DCM, respectively. As a result, the converter cannot switch between CCM2 and DCM directly.

From the expressions of the output power (14), (16), (19) and the boundaries (17), (20), the normalized output power versus the normalized phase-shift angle $D$ is plotted in Fig. 6. For a curve with a certain gain, the transferred power in the CCM2 and DCM modes is less than CCM1 mode, which agrees with the analysis in previous section. In Section II, this phenomenon is explained on a perspective of circuit operation at every stage rather than the equations or expressions, which is helpful to understand the characteristic of the converter. Therefore, CCM2 and DCM are suitable for the light-load conditions. Additionally,
Fig. 7. Primary currents with different phase-shift angles in a half switching period.

the areas of CCM2 and DCM modes are not adjacent, which is separated by CCM1 area.

As shown in Fig. 6, if the gain is smaller than 1, the output power cannot be reduced to zero even when the phase-shift angle is zero in CCM2. The secondary side works as a passive rectifier when the phase-shift angle is zero, while the primary side works like a traditional non-PSFB converter with 0.5 duty cycle. Thus, the power can still be transferred to the load if the output voltage is relatively low. This issue can be solved easily to make the proposed converter operate in the burst mode for the light-load applications.

Another potential feature is that the converter can provide the same output power with two different phase-shift angles for a certain gain. To explain this phenomenon, the waveforms of \( i_p \) in two scenarios during half of a switching period are illustrated in Fig. 7. In the two situations, the input voltage and the voltage gain are assumed to be the same. \( i_{p1} \) in the solid line has a small phase-shift angle \( \phi_1 \), while \( i_{p2} \) in the dotted line has a larger phase-shift angle \( \phi_2 \). Since most of the power is delivered at the power-transferring stage, the power is approximately proportional to the size of the shadowed rectangular area. If \( \phi \) increases, \( i_p \) at the power-transferring stage becomes larger while the duration of the stage is shortened. As a result, as the phase-shift angle changes, there are probably two situations where the shadowed areas are the same. That means there are two possible phase-shift angles for one certain output power.

In the practical applications, only the scenario with the smaller phase-shift angle is recommended because the primary and secondary currents are higher with the larger phase-shift angle \( \phi \). Fig. 8 illustrates the simulation result waveforms with 600-V input voltage, 96-V output voltage, and 1-kW rated output power. And the output power curves with three different input voltages 600, 720, and 800 V are plotted in Fig. 9. As shown in Fig. 8, although the converter can provide 1 kW with two different phase-shift angles 0.38 and 0.86, the peak primary current with the larger phase-shift angle is almost twice of that with the smaller phase-shift angle. Therefore, the left half white area in Fig. 9 with \( D \) less than 0.5 is recommended for the practical operation.

B. Soft-Switching Condition

1) Primary Switches: The ZVS turn-off of the primary switches is obtained due to the parallel capacitors. The larger the parallel capacitors are, the less turn-off losses would be caused. In the steady-state operation of CCM1 and CCM2, ZVS turn-on is achieved for all the primary power MOSFETs, which reduces the switching losses greatly. When \( S_{p1} \) and \( S_{p4} \) turn OFF, the inductor \( L_{Lk} \) charges \( C_{p1} \) and \( C_{p4} \), and discharges \( C_{p2} \) and \( C_{p3} \). As a result, the ZVS turn-on for the switches \( S_{p2} \) and \( S_{p3} \) can be realized once \( C_{p2} \) and \( C_{p3} \) are discharged completely. The condition for the ZVS turn-on of another pair of primary switches is the same. Fig. 10 shows the primary referred equivalent circuit when primary switches turn OFF. \( V_{cp} \) equals to 0.5\( V_{in} \) when the primary switches turn OFF. Since the output capacitor is relatively large, the output
voltage is assumed constant during this short duration. In the following expressions, the primary current is \( i_p(0) \) when \( S_{p1} \) and \( S_{p2} \) turn OFF. And \( V_{cp} \) could be expressed as

\[
V_{cp} = N V_{out} - A \cdot \sin(\omega t + \delta)
\]

where

\[
A = \sqrt{\left(N V_{out} - \frac{1}{2} V_{in}\right)^2 + Z^2 \cdot i_p(0)^2}
\]

\[
\delta = \arctan \left[ \frac{N V_{out} - \frac{1}{2} V_{in}}{Z \cdot i_p(0)} \right]
\]

\[
\omega = \frac{1}{\sqrt{L_{lk} \cdot C_p}}
\]

\[
Z = \sqrt{\frac{L_{lk}}{C_p}}.
\]

ZVS is achieved only if \( V_{cp} \) could reach \(-0.5V_{in}\) before the other pair of primary switches turn ON. As a result, the condition for ZVS in the CCM1 and CCM2 modes can be obtained as

\[
\frac{1}{2} L_{lk} \cdot i_p(0)^2 > \frac{V_{in}^2 \cdot G \cdot C_p}{2}.
\]

The condition is related to both the input and output voltages. That is because the leakage inductor energy is transferred to the load and the input terminal during this interval. So a higher output voltage consumes more energy and makes ZVS realization more difficult.

In addition, the dead time between the inner pair and the outer pair of primary switches should be set long enough to accomplish ZVS operation, which can be expressed as

\[
T_d > \frac{1}{\omega} \left( \arcsin \frac{N V_{out} + \frac{1}{2} V_{in}}{A} - \delta \right).
\]

In the DCM mode, ZVS is not assured since the primary current decreases to zero when the primary switches commutate, whereas, in case of a small magnetizing inductance of the transformer, the magnetizing current could facilitate ZVS of the primary switches. Unfortunately, a large magnetizing current could cause more conduction losses. Consequently, a tradeoff between the switching losses and conduction losses should be made.

2) Secondary-Side Switches: As analyzed in Section II, the ZVS of the secondary-side switches is achieved naturally in CCM1. No extra condition has to be satisfied for ZVS-on of the secondary-side switches. In CCM2, however, ZVS is lost because the secondary-side switch turns ON before \( i_s \) declines to zero.

In DCM, the primary current is not continuous, which may lead to the loss of ZVS. At time \( \theta_1 \) in Fig. 5, \( V_{ds} \) of \( S_{s1} \) is regulated by

\[
V_{s1} = \frac{1}{2} \frac{V_{in}}{N} \left[ 1 - \cos(\omega_1 t) \right] + i_s(\varphi) \cdot Z_1 \cdot \sin(\omega_1 t)
\]

where

\[
\omega_1 = \frac{1}{\sqrt{C_s \cdot L_{lk}/N^2}}
\]

\[
Z_1 = \sqrt{\frac{L_{lk}}{N^2 C_s}}
\]

where \( i_s(\varphi) \) is the current through the secondary winding of the transformer when \( S_{s1} \) turns OFF, \( C_s \) is the parallel capacitance of the secondary-side switch. That is, \( C_s = C_{s1} = C_{s2} \). In order to achieve ZVS, \( V_{s1} \) should reach \( V_{out} \) before \( S_{s2} \) turns ON. As shown in (28), if \( G < 2 \), the condition for ZVS is satisfied naturally even without the help of \( i_s(\varphi) \). Because \( L_{lk} \) and \( C_{s1} \) start resonating after \( S_{s1} \) turns OFF, \( V_{s1} \) can reach twice of the secondary-side referred input voltage \( V_{in}/2N \) when \( i_s(\varphi) \) equals zero. In case that \( G > 2 \), \( i_s(\varphi) \) should be larger than zero to charge \( C_{s1} \) completely. The energy of \( L_{lk} \) and the dead time should be regulated by

\[
i_s(\varphi) > \frac{V_{in} \sqrt{G^2 - 2G}}{2N \cdot Z_1}, \quad (G > 2)
\]

\[
T_{d1} > \frac{1}{\omega_1} \left[ \arcsin \frac{V_{in}(G - 1)}{\sqrt{4N^2 \cdot Z_1^2 \cdot i_s(\varphi)^2 + V_{in}^2}} \right. + \arctan \left. \frac{V_{in}}{2N \cdot Z_1 \cdot i_s(\varphi)} \right].
\]

The magnetizing current has an influence on efficiency of the converter because it may cause extra conduction losses in the primary side. Fortunately, due to the small value of the magnetizing current, the extra conduction losses are quite small compared with those generated by the normal primary current. Furthermore, the magnetizing current facilitates the ZVS operation of the primary switches, especially in the low-power conditions. This raises the circuit conversion efficiency.

C. Voltage Stress Analysis

Once ignoring the voltage ripple on the input capacitors, the voltage stress of the primary power switches is half of the input voltage, which means the low-voltage rated power devices with superior performance can be employed to reduce the conduction losses.

Since there is no filter inductor in the secondary rectifier circuit, the turn-off voltage across the secondary-side switches is clamped by the output voltage, and the voltage spikes on the switches are effectively suppressed. Therefore, the voltage stresses of the secondary-side switches including the MOSFETs and diodes are just the output voltage. The low-voltage rated MOSFETs and diodes could be adopted as the secondary-side power switches, which help the converter accomplish better performance.

IV. DESIGN GUIDELINES

A 1-kW 100-kHz prototype is established to be used as an example to give a clear parameter design procedure. In the tested prototype, the input voltage varies from 600 to 800 V and the output voltage is 96 V for the battery charging system.

A. Transformer Turns Ratio

The turns ratio is the key parameter because it determines the converter operation mode. The input voltage for the balance
mode should be a moderate one to minimize the switch current stress, which is selected as 720 V in this test bench. According to (1), the turns ratio can be designed.

B. Leakage Inductor

Based on (1), (14), (16), and (19), the practical output characteristic curve can be plotted in Fig. 9. The rated output power is denoted as a horizontal line which could be moved vertically in Fig. 9. To guarantee that the rated power can be transferred over the full range of input voltage, the rated power line should have crossing points with every output characteristic curve, especially with the lowest input voltage 600 V curve. Also, the position of the rated power line needs to be carefully chosen in order to have a proper working range of the phase-shift angle ϕ. Then, the percentage of \( P_b \) that the rated power is can be obtained on the \( y \)-axis of Fig. 9. And \( L_{Lk} \) can be calculated as

\[
L_{Lk} = \frac{(NV_{out})^2\varepsilon}{2\pi f_s P_r} \quad (33)
\]

where \( P_r \) and \( \varepsilon \) are the rated power and the percentage of \( P_b \) that the rated power is, respectively.

C. Dead Time

The dead time of the primary switches can be calculated from (23) and (27), while the dead time of the secondary switches can be obtained through (32).

D. Control Loop

The output voltage and transferred power are regulated by only directly varying the phase-shift angle \( \varphi \), which is generated through the digital signal processor according to the output characteristic curve shown in Fig. 6.

And the classical voltage feedback loop is adopted to regulate the output voltage in this experimental prototype. The difference between the voltage reference and the sampled output voltage goes through the PI compensator to the phase-shift generation block. Due to the updated phase-shift angle, the SSPS converter changes the output voltage. The PI compensator and phase-shift generation is completed by TI TMS320F2808. Actually, other advanced feedback control strategies can be also employed to improve the steady-state and dynamic response of the proposed converter [23].

V. EXPERIMENTAL VERIFICATIONS

A 1-kW 100-kHz prototype is established to verify the theoretical analysis. The specifications are listed in Table II. The input voltage is 600–800 V, and the output voltage is 96 V. The transformer turns ratio is 15:4, which means the converter works in the balance mode at the input voltage of 720 V ideally. IRFP460 and IRFP4668 are adopted as the primary and secondary switches, respectively. 30CPQ150 is selected as the secondary-side diodes. And the leakage inductor is designed to be 50 µH. The parallel capacitors of the primary and secondary switches are 470 pF and 1 nF, respectively. And a 4.7-µF CBB capacitor is selected as the primary block capacitor.

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{in} ) (Input voltage)</td>
<td>800 V</td>
</tr>
<tr>
<td>( V_{out} ) (Output voltage)</td>
<td>96 V</td>
</tr>
<tr>
<td>( P_{out} ) (Maximum output power)</td>
<td>1000W</td>
</tr>
<tr>
<td>( f_s ) (Switching frequency)</td>
<td>100 kHz</td>
</tr>
<tr>
<td>( N ) (Turns ration n/n2)</td>
<td>15/4</td>
</tr>
<tr>
<td>( L_{dk} ) (Primary transformer leakage)</td>
<td>50 µH</td>
</tr>
<tr>
<td>( S_{p1}, S_{p2} ) (Primary power MOSFETs)</td>
<td>IRFP460N</td>
</tr>
<tr>
<td>( S_{s1}, S_{s2} ) (Secondary power MOSFETs)</td>
<td>IRFP4668</td>
</tr>
<tr>
<td>( D_{s1}, D_{s2} ) (Output diodes)</td>
<td>30CPQ150</td>
</tr>
<tr>
<td>( C_{p1}\sim C_{p4} ) (Parallel capacitors of primary-side MOSFETs)</td>
<td>470 pF</td>
</tr>
<tr>
<td>( C_{s1}, C_{s2} ) (Parallel capacitors of secondary-side MOSFETs)</td>
<td>1 nF</td>
</tr>
<tr>
<td>( C_i ) (Block capacitor)</td>
<td>4.7 µF</td>
</tr>
<tr>
<td>( C_o ) (Output capacitor)</td>
<td>470 µF</td>
</tr>
</tbody>
</table>

Figs. 11–13 display the waveforms of the primary, the secondary-side switch, and the secondary-side diode with \( V_{in} = 800 \text{ V} \), \( V_{out} = 96 \text{ V} \) and \( P_{out} = 1 \text{ kW} \), respectively. With the parameters, the converter works in CCM1 mode with \( G < 1 \).

As shown in Figs. 11 and 12, ZVS is achieved for the primary-side active switch and the secondary-side switch. Since all the primary switches work in the same pattern and both the secondary-side switches work symmetrically, ZVS is accomplished for all the primary and secondary active switches. And due to the soft switching, there are no voltage spikes on the primary switch. It can be seen that the voltage stress of the primary switches is about 400 V, which is half of the input voltage.
As a result, the low-voltage rated power MOSFETs with high performance can be employed to reduce the conduction losses.

It can be seen from Figs. 12 and 13 that the voltage stresses of the secondary-side active switches and diodes are clamped to the output voltage 96 V. And the voltage spikes on both the secondary-side MOSFETs and diodes are effectively suppressed, since the output filter inductor is removed. Furthermore, there is no reverse recovery problem for the diodes, since the current falling rate of the output diode is controlled by the leakage inductance.

The three pairs of $v_p$ and $i_p$ waveforms in Fig. 14 are measured under the condition of 1-kW output power and different input voltages. It can be seen that the converter works in the CCM1 mode at all of the three situations. The primary current increases, remains constant, and declines linearly at the power-transferring stage in the buck, balance, and boost modes, respectively. Fig. 14(b) demonstrates the balance mode with $V_{in} = 730$ V, $V_{out} = 96$ V, and $N = 15/4$. The input-side ($V_{in}/2$) and output-side ($NV_{out}$) voltages of the leakage inductor are the same, considering the forward voltage of diodes and MOSFETs. So the primary current keeps constant at the power-transferring stage, which is in compliance with the theoretical analysis in Section II.

The waveforms of $v_p$ and $i_p$ in Fig. 15 are measured under the condition of 400-W output power and 600-V input voltage. The primary current decreases rapidly during the power-transferring stage with gain $G > 1$, which agrees with the above analysis. However, the primary current does not decrease to zero and begins increasing again after the power-transferring stage, which is not completely compatible with the analysis in Section II. Because the transformer magnetizing inductance is not infinitely large, the magnetizing current cannot be neglected. The output and input voltages are addressed on the transformer during and after the power-transferring stage, respectively. As a result, the magnetizing current begins increasing from zero since the power-transferring stage, and the primary current does not decrease to zero and begins increasing, as shown in Fig. 15.

As the output power varies from zero to the rated, the measured efficiency curves with respect to different input voltages are plotted in Fig. 16. The peak efficiency is over 96%, and the efficiency of 94% is achieved in a wide power range due to ZVS operation in a wide voltage range, low-voltage rate high-performance power device utilization and small circulating losses. It is demonstrated that the converter is an excellent candidate for the high input voltage applications.

In order to clearly illustrate the efficiency performance of the proposed converter, the typical primary phase-shift-controlled three-level converter is used as an example and compared. The qualitative loss distributions in both converters are summarized
in Table III. For the primary-side losses, the proposed converter has lower conduction losses because it has lower freewheeling current and there is no extra primary clamping diodes. For the secondary-side losses, the reverse-recovery losses for the output diodes that exist in the conventional phase-shift converters are minimized due to the SSPS scheme. Furthermore, the output diodes in the conventional primary phase-shift-controlled converter suffer higher voltage stress compared with the proposed secondary-side phase-shift converter, which leads to larger conduction losses for the output diodes [17]. As a result, the proposed converter has higher efficiency than the conventional three-level converter. And it is also proved that the proposed converter has some superior performance from the data in [17].

The operation principle of the proposed converter is quite similar to that of the introduced circuit in [19]. However, in the 800-V or higher input voltage applications, due to the full-bridge configuration in [19], insulated-gate bipolar transistors should be employed to sustain the high bus voltage, which results in large conduction losses. Furthermore, the switching frequency is limited to impact the power density. This means a large and costly magnetic core should be selected for the transformer. In conclusion, in the high input voltage systems, the conversion efficiency and circuit cost of the proposed converter are a little competitive than those of the topology introduced in [19].

VI. CONCLUSION

In this paper, a secondary-side phase-shift-controlled ZVS dc/dc converter for high-efficiency, wide conversion range and high input voltage applications has been proposed and analyzed. The improved three-level configuration in the primary side halves the primary power devices, which makes it possible to employ low-voltage rated power switches for high input voltage applications. Furthermore, the ZVS can be achieved for all the power devices including the primary and secondary switches to effectively reduce the switching losses. Moreover, the circulating current is effectively suppressed due to the secondary-side phase-shift control scheme, which largely improves the efficiency of the converter. And the overshoots on the secondary-side devices are effectively suppressed by clamping the rectifier to the output voltage. In addition, a wide conversion range can be achieved since the converter can work in three modes including the buck, balance, and boost modes. The circuit operation and characteristics of the proposed converter is analyzed and simulated. Experimental results of an 800-V-96-V/1-kW prototype have verified the feasibility and effectiveness of the advantages of the proposed converter.

REFERENCES


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