A 284-μW 1.85-GHz 20-Phase Oscillator
Using Transfer Gate Phase Couplers

Hyeokjong Lee, Takashi Takeuchi, Masahiko Yoshimoto, and Hiroshi Kawaguchi

Department of Computer and Systems Engineering, Kobe University
1-1, Rokkodai, Nada, Kobe 657-8501, Japan
hyeok@cs28.cs.kobe-u.ac.jp

Abstract — We propose a transfer gate phase coupler for a low-power multi-phase oscillator (MPOSC). The phase coupler is an nMOS transfer gate, which does not waste charge to the ground and thus achieves low power. The proposed MPOSC can set the number of outputs to an arbitrary number. The test circuit in a 180-nm process and a 65-nm process exhibits 20 phases, including 90° different angles. In a 65-nm process, the measured peak DNL and 3σ period jitter are, respectively, less than ±1.2° and 5.82 ps. The minimum I/Q angle error is 0.019°. The power is 284 μW at 1.85 GHz.

Index Terms — multi-phase oscillator, transfer gate phase coupler, low-power, process scaling

I. INTRODUCTION

Ring oscillators, which output multiple phases, are widely used in signal processing. Particularly, multiple phases with a small clock skew ring oscillators are used: the high-resolution phases enable writing to optical disks [1-3].

There are three methods for generating multiple phases. First, a ring oscillator consists of multiple-stage inverter. This method is very simple. But, it cannot generate multiple phases with high frequency. Second, multiple phases are generated by a LC-VCO with phase interpolator. The method has lower-power consumption and higher resolution than ring oscillator. Unfortunately, it has a narrow-band frequency for LC-VCO with high Q. Another way is to use phase coupled inverter chain which is made from multi-phase oscillator (MPOSC) [1-4]. High frequency with wide-band outputs can be achieved using the MPOSC. However, the conventional inverter-structured and latch-structured phase couplers shown respectively in Figs. 1 (b) and (c) draw the charge to the ground, which means the phase couplers consume unnecessary power themselves [1-2].

In this paper, we propose to adopt a transfer gate phase coupler (TGPC) that wastes no charge to the ground which enable a low-power MPOSC. By using the TGPC, we can set the number of inverter chains to an even number. We also explain the charge operation of TGPC in MPOSC implement TGPCs in 180-nm and 65-nm processes, and it is confirmed that the TGPC possesses process scalability.

II. CONVENTIONAL PHASE COUPLER

The MPOSC consists of coupled inverter chains. In other words, the frequency and the phases are defined respectively by inverter chains and phase couplers. Those are made to one ring, where phase couplers are link to other rings. For instance, a 5×5 MPOSC consists of five inverter chains of five stages and 25 phase couplers. Here, inverter chains turn out to be oscillated independently if assuming MPOSC has not the phase couplers. The phase couplers derive accurate phases from the coupled inverter chains.

The current-controlled conventional MPOSC is shown in Fig. 1, with two kinds of phase couplers. The inverter-structured phase coupler does full-swing of charge between inverter chains. For this reason, oscillation frequency depends on not only inverter chains but also the ring of phase couplers. Thus, in acquisition of a lot of phases, the ring delays larger and there is a limit of oscillation frequency.

Another conventional approach is a latch-structured phase coupler. The latch of two nMOS does half-swing of charge between inverter chains. Although phase couplers have the relation, it is not restrained like the inverter coupler. Oscillation frequency depends on only inverter chains, and it can oscillate at higher frequency.

In this way, the conventional MPOSCs consume power for swing of charge between inverter chains. When nMOS of the inverter-structured phase coupler is turned on, it discharges through inverter. The latch-structured phase coupler does so. The conventional phase coupler draws current to the ground through itself and consumes power even if the MPOSC is locked. Thereby, the conventional MPOSC wastes more power than the ring oscillator composed of the same number of stages.

We explain a 5×5 MPOSC with the inverter phase coupler in detail using Fig. 2. As for this MPOSC, P1 is connected to input of the phase coupler, and its output (P14) is connected to output of another phase coupler. The nMOS or pMOS of the phase coupler becomes active by the P1 state. When the
nMOS becomes active, $P_{14}$ is discharged. On the other hand, when the pMOS becomes active, $P_{14}$ is charged. When $P_{14}$ was delayed, it is discharged by the nMOS of phase coupler (on the rising edge, $P_{14}$ will be charged after the pMOS becomes active). In contrast, when $P_{14}$ was advanced, it is locked for the same reason.

III. TRANSFER GATE PHASE COUPLER

Now, $m$ sets of $n$-stage ring oscillators in Fig. 1 are considered. A phase differences of the MPOSC outputs are the following equation.

$$\frac{360^\circ}{m \times n} = P_{\text{res}}$$  \hfill (1)

In that equation, $P_{\text{res}}$ is a phase resolution; $n$ is limited to an odd number and must be larger than three for a ring oscillator. Because the inverter or latch in Figs. 1 (b) or (c) is used as a phase coupler in the conventional MPOSC, it inverts a phase signal, which means that $m$ must be an odd number, too; otherwise, the ring is stabilized and is not oscillated.

In contrast, our MPOSC scheme adopts the nMOS transfer gate presented in Fig. 3; it does not accompany the inverting operation as a phase coupler. Consequently, the proposed scheme can accommodate setting of $m$ to an arbitrary number.

For instance, the minimal components that create I/Q signals (90°-differential signal) are $m = 4$ and $n = 3$ in our MPOSC. In the practical design, we chose $m = 4$ and $n = 5$ ($P_{\text{res}} = 18^\circ$) by increasing the number of stages in the inverter chain for finer phase resolution and lower jitter. A $72^\circ$ delayed signal is used to turn on an nMOS TGPC. A detailed schematic of our proposed design is presented in Fig. 4.

The proposed TGPC uses nMOSes controlled by the outputs of the inverter chains. The waveforms of the proposed TGPC, which further explain the operation principle, are portrayed in Fig. 5. In fact, $P_4$ and $P_8$ are derived from the same ring oscillator as shown in Fig. 3. Their mutual phase relation is a stable $72^\circ$, which is applied to the phase coupler control. Because of the stable $72^\circ$ difference in the phase between $P_4$ and $P_8$, $P_8$ always turns on the nMOS TGPC at $P_4$’s falling edge. The TGPC draws the current from $P_4$ to $P_8$ if they are not locked.

Fig. 3. The proposed multi-phase oscillator schemes.

Fig. 4. Detailed schematic of the proposed multi-phase oscillator.
Fig. 5. Principle of the transfer gate phase coupler.

For that reason, $P_3$ will be locked. The TGPC using $P_4$ and $P_8$ can determine the $P_3$’s phase. Once $P_3$ and $P_4$ are locked, the current flows less because the voltage difference between them is quite small. The current is decreased with the increase of a phase number because the different voltage becomes smaller. Consequently, our proposed MPOSC is highly effective for developing the oscillation; the TGPC’s power overhead can be minimized.

IV. MEASUREMENT RESULTS

This section describes VLSI implementation and measurement results.

A. Chip implements

The output from the four sets of five-stage ring oscillators is 20 phases, including I/Q signals. Fig. 6 portrays a chip layout of the proposed MPOSC core in a 180-nm and 65-nm CMOS process technologies. The respective core areas are $40.6 \times 54.2 \mu m^2$ and $15.92 \times 7.69 \mu m^2$, including the level shifters that drive the external source followers. These results show that the proposed MPOSC has process scalability and that its chip area can be reduced through process scaling.

<table>
<thead>
<tr>
<th>Process</th>
<th>Output frequency</th>
<th>Phase resolution</th>
<th>DNL of output phase</th>
<th>Period jitter($3\sigma$)</th>
<th>Accumulation jitter($3\sigma$) (100 clocks)</th>
<th>Power consumption</th>
<th>Core size</th>
</tr>
</thead>
<tbody>
<tr>
<td>180-nm CMOS</td>
<td>120 – 581 MHz</td>
<td>$T/20 (&gt;=86 \text{ ps})$</td>
<td>$-1.30^\circ \text{ to } 1.50^\circ$ @ 581 MHz</td>
<td>12.0 ps @ 581 MHz</td>
<td>26.3 ps</td>
<td>920 $\mu W$ @ 581 MHz</td>
<td>$40.6 \mu m \times 21.3 \mu m$</td>
</tr>
<tr>
<td>65-nm CMOS</td>
<td>0.024 – 185 GHz</td>
<td>$T/20 (&gt;=27 \text{ ps})$</td>
<td>$-1.22^\circ \text{ to } 0.86^\circ$ @ 1.85 GHz</td>
<td>5.82 ps @ 1.85 GHz</td>
<td>12.8 ps</td>
<td>286$\mu W$ @ 1.85 GHz</td>
<td>$15.92 \mu m \times 7.69 \mu m$</td>
</tr>
</tbody>
</table>

Fig. 7. Measured waveforms and period jitter in 180-nm process.

Fig. 8. Measured waveforms and period jitter in 65-nm process.

B. Performances

The result measurement of the 180-nm and 65-nm CMOS process technologies are shown in TABLE I. We have confirmed that the oscillating frequencies in the processes respectively achieve 581 MHz at a supply voltage of 1.8 V and 1.85 GHz at a supply voltage of 1.2 V. The measured $3\sigma$ period jitter in the 180-nm node is 12.0 ps at 581 MHz, and that in the 65-nm node is 5.82 ps at 1.85 GHz. Figs. 7 and 8 shows waveforms from source followers as measured examples ($P_3$ and $P_4$: 18° different).
the maximum DNL is less than ±1.2° and the minimum I/Q angle error is 0.019°.

In the 180-nm CMOS process, a comparison of the power-delay (PD) products between the conventional MPOSCs and the proposed MPOSC is depicted in Fig. 10. The results show that the proposed MPOSC with the TGPCs is superior to the other MPOSCs. As the phase number increase, it becomes more effective in power. It is comparable to the ring oscillator that does not use phase coupling. We observed that 36.6% and 38.3% improvements can be achieved, respectively, compared with the conventional MPOSCs with the inverters and nMOS latches.

![Fig. 9. Measured DNL and I/Q DNL of the phases.](image)

![Fig. 10. Comparison of PD products of MPOSCs and ring oscillator.](image)

Fig. 10. Comparison of PD products of MPOSCs and ring oscillator.

Fig. 11 confirmed the process scalability of the 180-nm CMOS process and the 65-nm CMOS process. The PD product when setting oscillation frequency to 450 MHz is measured. It is understood that the proposed TGPC oscillator is superior to the conventional MPOSC in low-power consumption. In particular, when the same frequency is set in each process, the source voltage can be lower by scaling. As a result, we confirmed that the PD product can be made lower than that in the conventional one by this measure.

![Fig. 11. Shift of PD products with process scaling.](image)

V. CONCLUSION

In this paper, we propose a low-power MPOSC with single-end inverters and the TGPCs. It can set the number of inverter chains to an arbitrary number. We have implemented the proposed MPOSCs in a 180-nm CMOS process and a 65-nm CMOS process, which respectively consumed power of 920 μW at 581 MHz and 286 μW at 1.85 GHz, indicating that our proposed MPOSC is suitable for process scaling.

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