IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.Doi Number

A 16-bit 1-MS/s Pseudo-Differential SAR ADC with Digital Calibration and DNL Enhancement Achieving 92 dB SNDR

Panpan Zhang[1,2], Wenjiang Feng[1], and Peng Zhao[2], Xiaoping Chen[2], Zongjiang Zhang[2]

[1] College of Microelectronics and Communication Engineering, Chongqing University, Chongqing 400044, China
[2] Shenzhen State Micro Electronics Co.,Ltd. Shenzhen, China

Corresponding author: Panpan Zhang (e-mail:ppzhang1@ssmec.com).

This work was supported in part by the Chongqing Basic Science and Frontier Technology Research Project (cstc2017jcyjBX0047).

ABSTRACT This paper presents a 16-bit 1 MS/s pseudo-differential Successive-Approximation-Register Analog-to-Digital Converter (SAR ADC) achieving an ENOB of 15-bit. To accommodate the pseudo-differential input, a differential DAC utilizing both monotonic and traditional switching is designed. For both dynamic and static performance improvement, three techniques are proposed. First, a foreground digital self-calibration method is described to eliminate the capacitor mismatch errors. Some of the LSBs capacitors are utilized to measure and calculate the bit weights of other capacitors. Second, a DNL enhancement technique is presented. The fractional value capacitors are used to subtract an analog voltage from the DAC before the conversion is finished, which cancels out the consequent effect when the fractional part of the digital output is discarded before final output. Third, a low-offset low-noise comparator is designed. A reset timer with DAC settling replica is proposed to make the pre-amplifier in the comparator to start to amplify the DAC summing node voltage right after the DAC has fully settled. A prototype ADC is fabricated in a 0.18-μm 5-V CMOS process. It measures a 92.3-dB SNDR and a 107.9-dB SFDR. The DNL and INL are within ±0.3 LSB and ±0.72 LSB, respectively. The overall power consumption, drawn from the 5 V power supply, is 40 mW.

INDEX TERMS Successive-Approximation-Register Analog-to-Digital Converter (SAR ADC), Digital Calibration, Pseudo-Differential, DNL enhancement

I. INTRODUCTION

High-resolution successive-approximation-register analog-to-digital converters (SAR ADC) with several hundreds of kS/s or several MS/s are extensively used in industrial measurement, medical instruments, and battery-powered systems due to its simple structure and low power. Compared with its counterpart Σ-Δ ADC, SAR ADC has an edge in its capability to handle multiplexed inputs on chip and small latency, making it a popular ADC architecture in data acquisition system.

Generally speaking, there are three input types for ADC: fully differential, pseudo-differential, and single-ended, as shown in Fig. 1. The fully differential is the most common one because it provides the best common mode noise rejection ratio and doubles the input dynamic range. However, in many of the application environments for high-precision SAR ADC, the original data to be sampled are single-ended. Converting such signal to differential form on board increases the system complexity and area. Under such situations, pseudo-differential input type can be utilized. The positive input connects to the actual signal and

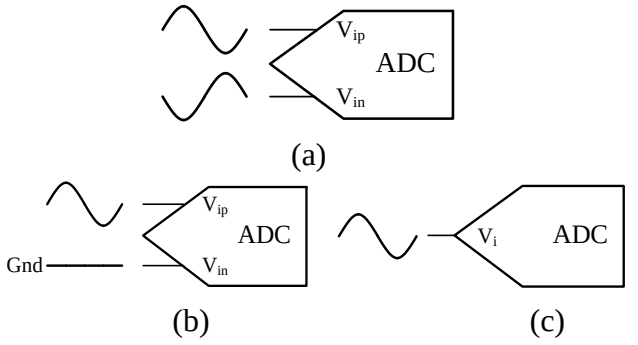


FIGURE 1. ADC input types (a) fully differential; (b) pseudo-differential; (c) single-ended.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

the negative input senses the signal ground which is separated from the ADC ground. This is useful especially when the signal plane is far away from the ADC. The third input type is single-ended. It is the simplest one but provides no extra benefits. In this paper, a 16-bit pseudo-differential SAR ADC with redundancy is introduced.

For charge redistribution SAR ADC with resolution larger than 12 bits, calibration is necessary to eliminate the mismatch errors of the capacitors. Some known calibration methods use an extra DAC to measure and compensate the capacitor mismatch in analog domain[1][2][3], but they only apply to binary DAC and the extra DAC increases the power and area of analog circuits. In recent years, as nano-meter CMOS process is used for SAR ADC design, digital background calibration techniques are proposed. Either least-mean square (LMS) algorithm[4][5][6] or PN signal correlation[7][8][9] is used to find the digital bit weights, but these methods rely on the input signal. Some specific kinds of input, such as square wave, DC, or very small amplitude input, may corrupt the calibration.

A digital self-calibration method works in foreground is introduced in this paper. The mismatch errors of higher bits capacitors are measured by the lower bits, and the results are used to calculate their digital bit weights which are stored and accumulated during normal conversion. The SAR logic in calibration, including the redundant bits, is designed to be identical with that in normal conversion, so as to simplify the logic circuits.

Based on the digital bit weight calibration, a DNL enhancement technique is proposed in this paper to further improve the ADC performance by utilizing the fractional part of the accumulated output codes.

Another major issue to be considered is that the foreground digital calibration requires the comparator offset to be eliminated. Meanwhile, a 16-bit SAR ADC targeting a SNDR above 90 dB demands a very low noise comparator. Details on the circuit topology and analysis of the low-offset low-noise comparator will be given later.

The overall ADC architecture, including the pseudo-differential DAC, comparator with offset cancellation, calibration control module, SAR, and calibration logic, is shown in Fig. 2. The rest of the paper is organized as follows. Section II describes the architecture and switching method of the pseudo-differential DAC with redundancy. Section III and Section IV include the digital self-calibration and DNL enhancement technique respectively. The design details of the comparator are given in Section V. Finally, the measurement results are shown in Section VI.

II. PSEUDO-DIFFERENTIAL DAC

A. DAC STRUCTURE

As shown in Fig. 2, the input signal is sampled onto the P-side DAC, whereas the N-side DAC senses the signal ground.

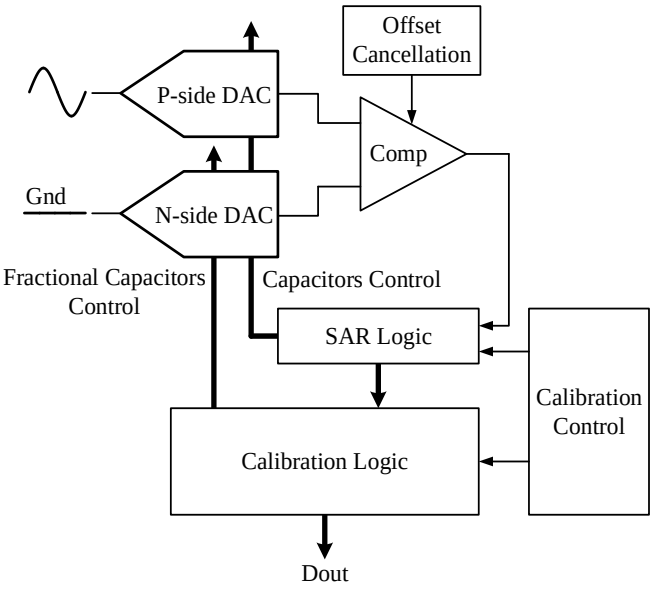


FIGURE 2. Overall ADC architecture.

The capacitor array, depicted in Fig. 3, is identical for both sides. To save chip area, the capacitor array is divided into 13-bit and lower 7-bit with 4 bits redundancy. The first two redundancy bits are designed to correct previous wrong decisions which may be caused by reference bouncing or DAC incomplete settling. Because the capacitors must be large enough to suppress the sampling noise and the bandwidth of the pre-amplifier in the comparator must be small enough to suppress the comparator noise, settling is still of a concern. The third redundancy bit, located at the LSB capacitors array, is included in case that the coupling capacitor C_C is much smaller than the designed value. Under that situation, there may be no redundancy for C_{13} and the lower bits value during conversion would be all 0s or all 1s. Although C_C is already sized 5% larger than ideal, we still include this redundancy bit to be more "safe" as C_C is not a unit capacitor and its mismatch is not well controlled. The last redundant bit C_{19} is mainly used for DNL enhancement. It provides some redundancy after the fractional part of the digital output is subtracted from the DAC. Details on this issue will be explained in Section IV. The fractional capacitors C_{21} to C_{25} are designed for digital calibration and DNL enhancement.

During sampling, the bottom plates of C_1 to C_8 connect to the input signal, and the top plate connects to ground. Choosing ground as the top plate sampling voltage, rather than common mode V_{CM}, provides several benefits. First, V_{CM} generation circuit consumes extra power and a large decouple capacitor needs to be used. Second, unlike V_{CM} sampling, bootstrap circuit is not needed to sample the ground. Finally, a separate ground, not used for any other analog or digital circuits, is the clearest and easily obtained signal for sampling.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

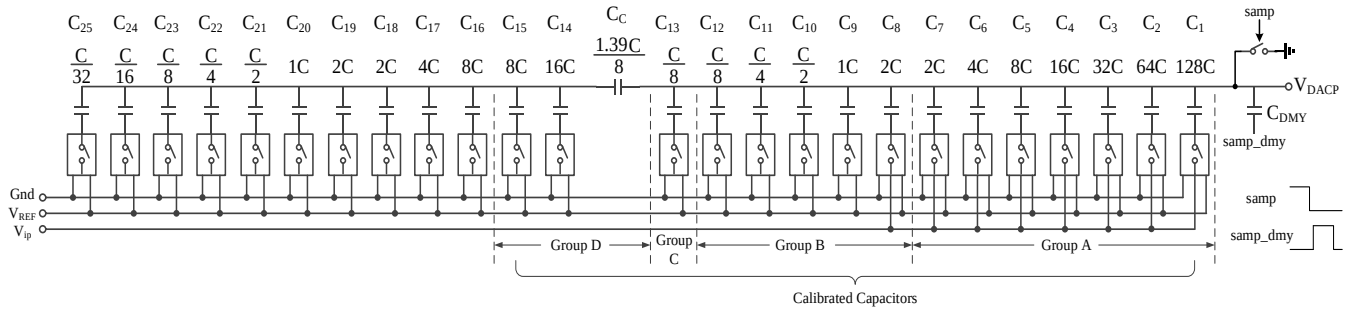


FIGURE 3. DAC capacitor array.

However, a problem that needs to be considered is that the DAC top plate voltage would drop to below 0 V due to the coupling of the falling edge of the sampling clocks connecting to both the top and bottom sampling switches. The total gate-to-drain capacitance of these switches, including the intrinsic capacitance of MOS device and layout parasitic, can be as large as 900fF in the worst case. Moreover, considering that the power supply may be 10% larger than ideal (5.5V), a voltage drop larger than 200mV can be observed from simulation. Although 200mV is not large enough to completely turn on the source-body PN junction of the top plate switch, a dummy capacitor C_{DMY} is connected to the DAC, as shown in Fig. 3, to avoid any potential charge leakage. The clock rising edge immediately after the sampling point at the bottom plate of C_{DMY} raises the DAC voltage to prevent it from dropping below zero.

B. SWITCHING METHOD

The detailed capacitor switching sequence is shown in Fig. 4. During the sampling phase, C_{1P} to C_{8P} connect to the input signal which ranges between 0 and V_{REF}. These capacitors switch to V_{REF} during the hold phase to make the summing node voltage of the P-side DAC limited between 0 and V_{REF}. The N-side DAC operates similarly as the P-side except that the MSB capacitor C_{1N} switches to ground in the hold phase to set the summing node voltage of the N-side DAC to be V_{CM} (V_{REF}/2). Meanwhile, C_{9P}, C_{14P}, C_{17P}, and C_{20P} switch to V_{REF} in the hold phase for the redundant bits switching and the corresponding capacitors in the N-side DAC operates the same to cancel the offset.

After that, the comparator makes the first decision. In the 1st bit cycle, according to the comparator output b_1, MSB capacitor of P-side C_{1P} switches to ground or maintains at V_{REF}, while the MSB-1 capacitor of N-side C_{2N} always switches to ground. Then, the comparator generates b_2. The similar procedure repeats 5 times. In the 6th bit cycle, C_{6P} switches to ground or maintains at V_{REF} according to b_6, while both C_{7N} and C_{8N} switch to ground simultaneously, which makes the voltage of N-side DAC return to 0 V. Meanwhile, C_{8P} also switches to ground to cancel the effect of the activity of C_{8N}. Thus the DAC differential voltage changes in the same pattern during the first 6-bit cycles.

From then on, the N-side DAC maintains static. During the 7th bit cycle, C_{7P} is controlled by b_7, C_{8P} switches to V_{REF} and C_{9P} switches to ground. During the 8th bit cycle, C_{8P} is controlled by b_8 and C_{9P} switches to V_{REF}. Through these activities, the P-side DAC voltage may increase or decrease by $V_{REF}\times C_9/C_{TOT}$ for two successive bit cycles if $b_7=b_8=1$ or $b_7=b_8=0$, where C_{TOT} is the total capacitance of the higher bits capacitor array. This is exactly how the redundant bit contributes to correcting the conversion errors happening before it.

After that, as can be seen in Fig. 4, the switching method actually follows the way of traditional SAR ADC except those redundant bits.

During the first 6-bit cycles, only monotonic switching using NMOS is involved, which helps to increase the speed as these capacitors are larger than others. Although the common mode voltage keeps decreasing from V_{REF}/2 to ground during these cycles, the dynamic offset of the comparator can be ignored because we have a cascode tail current source for the pre-amplifier. Moreover, the current source always works in saturation region since the power supply is 5 V which provides enough voltage headroom. As mentioned in [10], the offset variation of an amplifier is directly related to the variation of the override voltage of the input pair. With a cascode tail current source, the override voltage almost keeps a constant regardless of the input common mode, and therefore the dynamic offset of the comparator is small[10][18]. From simulation, the comparator offset variation with the common mode voltage sweeping from V_{REF}/2 (2.5 V) to ground is less than 110 μV, which can be well covered by the first redundancy bit.

III. DIGITAL SELF-CALIBRATION

A. BASIC PRINCIPLE

The calibration proposed in this paper uses the digital bit weights of lower bits capacitors to express those of higher bits. This is feasible because in the redundant DAC designed in Fig. 3, for i < 17, dw_i is guaranteed to be smaller than $\sum_{j=20}^{i+1} dw_j$,where dw_i is the digital bit weight of the ith capacitor. The calibration is similar to that in [16], but there are two major differences. First, we don't need to generate

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

	P-side DAC														N-side DAC													
	1.39/8 C	C_{13P}	C_{12P}	C_{11P}	C_{10P}	C_{9P}	C_{8P}	C_{7P}	C_{6P}	C_{5P}	C_{4P}	C_{3P}	C_{2P}	C_{1P}	C_{1N}	C_{2N}	C_{3N}	C_{4N}	C_{5N}	C_{6N}	C_{7N}	C_{8N}	C_{9N}	C_{10N}	C_{11N}	C_{12N}	C_{13N}	1.39/8 C
		C/8	C/8	C/4	C/2	1C	2C	2C	4C	8C	16C	32C	64C	128C	128C	64C	32C	16C	8C	4C	2C	2C	1C	C/2	C/4	C/8	C/8	
sampling		0	0	0	0	0	Vip	Vip	Vip	Vip	Vip	Vip	Vip	Vip	Vin	Vin	Vin	Vin	Vin	Vin	Vin	Vin	0	0	0	0	0	
hold		0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	
	(1)	0	0	0	0	1	1	1	1	1	1	1	1	1/0	0	0	1	1	1	1	1	1	1	0	0	0	0	
	(2)	0	0	0	0	1	1	1	1	1	1	1	1/0	1/0	0	0	0	1	1	1	1	1	1	0	0	0	0	
	(3)	0	0	0	0	1	1	1	1	1	1	1/0	1/0	1/0	0	0	0	0	1	1	1	1	1	0	0	0	0	
	(4)	0	0	0	0	1	1	1	1	1	1/0	1/0	1/0	1/0	0	0	0	0	0	1	1	1	1	0	0	0	0	
	(5)	0	0	0	0	1	1	1	1	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	1	1	1	0	0	0	0	
conversion	(6)	0	0	0	0	1	0	1	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0	1	0	0	0	0	
	(7)	0	0	0	0	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0	1	0	0	0	0	
	(8)	0	0	0	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0	1	0	0	0	0	
	(9)	0	0	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0	1	0	0	0	0	
	(10)	0	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0	1	0	0	0	0	
	(11)	0	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	0	0	0	0	0	0	0	0	1	0	0	0	0	

	C_{20P}~C_{25P}															C_{20N}~C_{25N}												
	C/32	C/16	C/8	C/4	C/2	1C	2C	2C	4C	8C	8C	16C	1.39/8 C	C_{13P} C/8	C_{12P} C/8	C_{12N} C/8	C_{13N} C/8	1.39/8 C	C_{14N} 16C	C_{15N} 8C	C_{16N} 8C	C_{17N} 4C	C_{18N} 2C	C_{19N} 2C	C_{20N} 1C	C/2	C/4	C/8	C/16	C/32
sampling	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0
hold	0	0	0	0	0	1	0	0	1	0	0	1		0	0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
(12)	0	0	0	0	0	1	0	0	1	0	0	0		1	1/0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
(13)	0	0	0	0	0	1	0	0	1	0	0	1		1/0	1/0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
(14)	0	0	0	0	0	1	0	0	1	0	1	1/0		1/0	1/0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
(15)	0	0	0	0	0	1	0	0	0	1	1/0	1/0		1/0	1/0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
conversion (16)	0	0	0	0	0	1	0	0	1	1/0	1/0	1/0		1/0	1/0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
(17)	0	0	0	0	0	1	0	1	1/0	1/0	1/0	1/0		1/0	1/0	0	0		1	0	0	1	0	0	1	0	0	0	0	0
(18)	0	0	0	0	0	0	1	1/0	1/0	1/0	1/0	1/0		1/0	1/0	0	0		1	0	0	1	0	0	1	1/0	1/0	1/0	1/0	1/0
(19)	0	0	0	0	0	1	1/0	1/0	1/0	1/0	1/0	1/0		1/0	1/0	0	0		1	0	0	1	0	0	1	1/0	1/0	1/0	1/0	1/0

FIGURE 4. Capacitors switching sequence.

two sets of output codes when calibrating one capacitor, which simplify the calibration process. Second, in [16], the offset is cancelled by applying an appropriate amount of offset using the dither capacitors. However, these dither capacitors are reused and they are also involved in the bit weight calibration, which makes the control of these dither capacitors complicated. In our calibration scheme, the offset is cancelled by another side of the differential DAC, or N-side DAC, while the capacitor switching method in the P-side DAC remains the same as in normal conversion. The overall control logic is thus quite simplified.

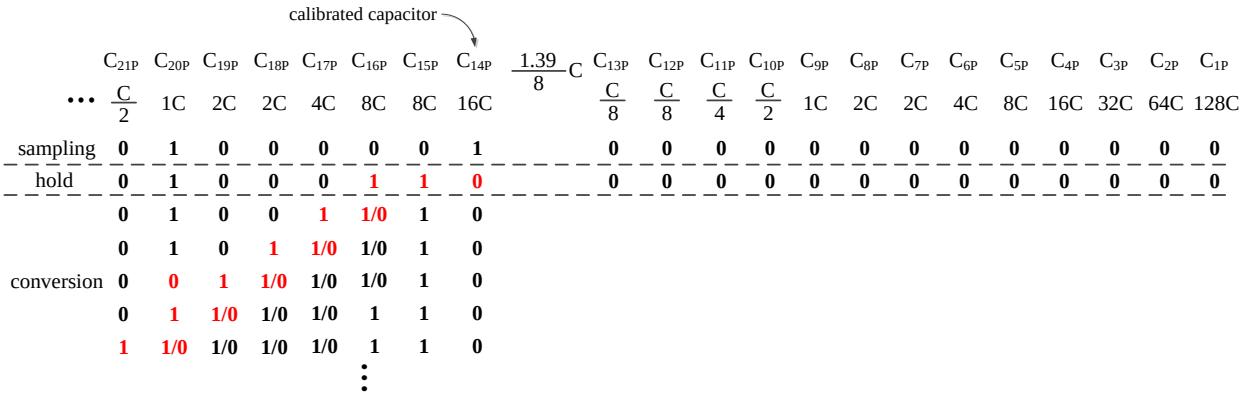
The capacitors to be calibrated are C_1 to C_{15}, which are calibrated one by one in sequence from C_{15} to C_1. They are divided into four groups as shown in Fig. 3. The capacitor switching method during calibration is depicted in Fig. 5. One capacitor in each group is chosen as an example. For instance, when C_6 is in calibration, it is connected to V_{REF} during sampling. Meanwhile, other capacitors except C_{14}, C_{17}, and C_{20} are connected to ground. Then, C_6, C_7, and C_8 switch to opposite direction during the hold phase. Ideally, C_6 is equal to the sum of C_7 and C_8, and therefore the DAC summing node remains at ground. Any mismatch between them causes a deviation from 0 V, which is then quantized using C_8 to C_{25}. As can be seen from Fig. 5, the capacitor switching is the same as that shown in Fig. 4, except that the starting point of SAR logic depends on which capacitor is under calibration. Similar ideas are applied to the calibration of other capacitors.

The calibration of C_{13} follows a slightly different way. Ideally, it is equal to the sum of C_{14} to C_{16}. Considering that C_C is a fractional value capacitor and thus its mismatch may be much larger than other unit capacitors, it is intentionally sized larger to guarantee enough redundancy for C_{13}. Therefore, the bit weight of C_{13} is smaller than the sum of the bit weights of C_{14} to C_{16} at the first place. To avoid the calibration overflow, during the hold phase, only C_{14} and C_{15} switch oppositely with respect to C_{13}. In other words, C_{13} is compared with C_{14} and C_{15} and their difference is then quantized.

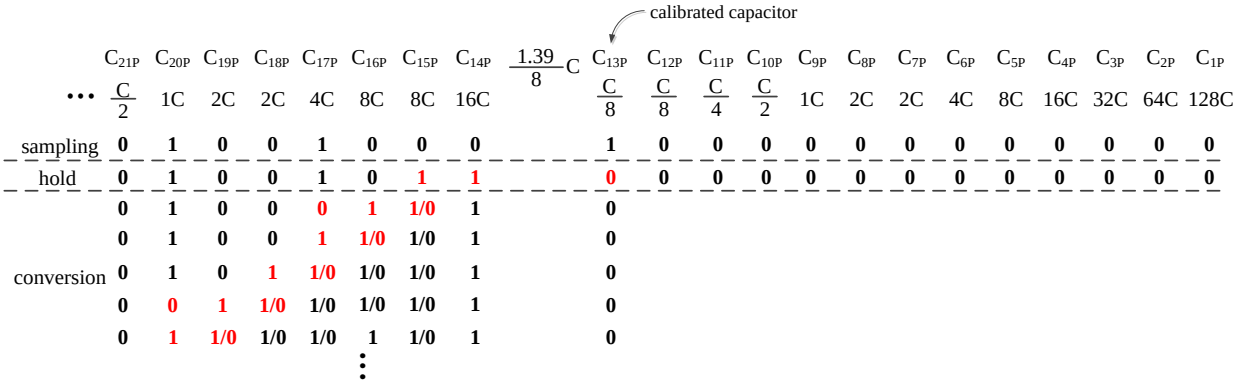
After the SAR logic is finished, some digital post-processing needs to be done. To illustrate the principle, V_X and V_Y are used to represent the summing node voltage of higher bits and lower bits CDAC, respectively. During sampling, V_X = 0 V. After the quantization is done, V_X successively approaches 0 V again. For V_Y, suppose V_Y = $V_{Y,samp}$ during sampling and V_Y = $V_{Y,conv}$ at the end of conversion.

Assume that C_i in group A is under calibration, and then the total charges on the two CDACs during sampling can be written as (1), where $C_{j,REF,samp,low}$ is the capacitor which

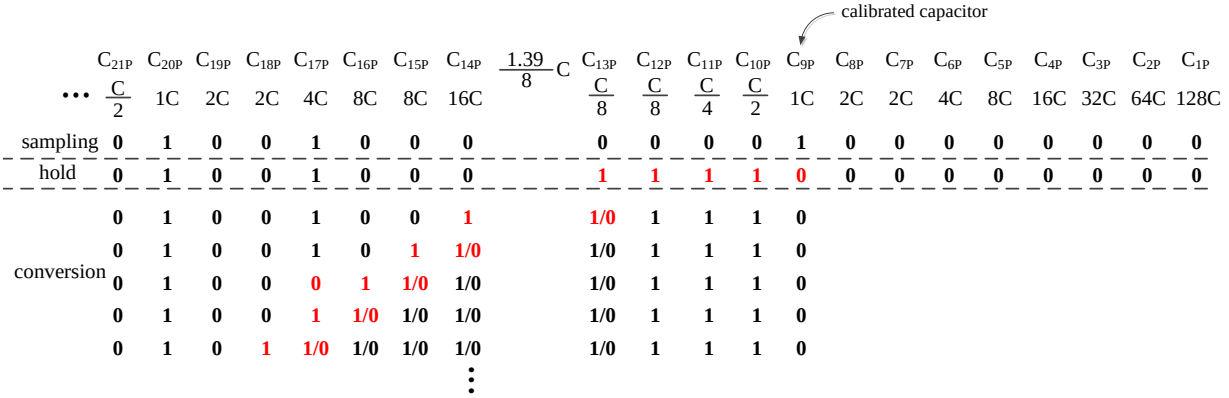
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access



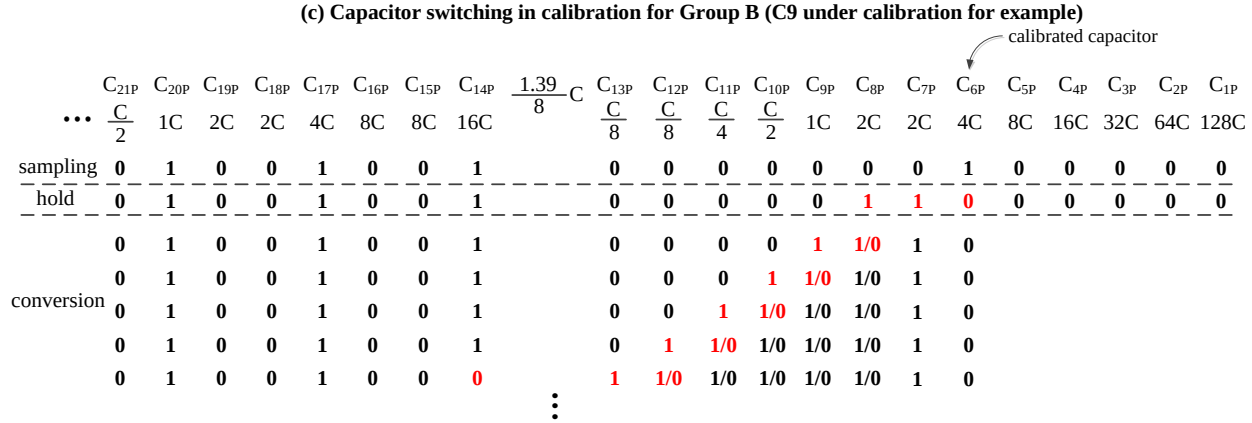
(a) Capacitor switching in calibration for Group D (C14 under calibration for example)



(b) Capacitor switching in calibration for Group C (C13 under calibration)



(c) Capacitor switching in calibration for Group B (C9 under calibration for example)



(d) Capacitor switching in calibration for Group A (C6 under calibration for example).

FIGURE 5. Capacitors switching in calibration.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

connects to V_{REF} during sampling in the lower bits CDAC (j = 14, 17 and 20 under this assumption), and $C_{TOT,LSB}$ is the total capacitance of lower bits CDAC.

At the end of conversion, the total charges change to $Q_{X,conv}$ and $Q_{Y,conv}$, as shown in (2), where $C_{j,REF,conv,high}$ and $C_{j,REF,conv,low}$ are the capacitors which connect to V_{REF} after conversion in the higher bits CDAC and lower bits CDAC, respectively.

According to charge conservation, $Q_{X,samp} = Q_{X,conv}$ and $Q_{Y,samp} = Q_{Y,conv}$. The value of C_i can be then derived as (3).

Dividing the above equation by $C_{TOT,MSB}+(C_{TOT,LSB}C_S)/(C_{TOT,LSB}+C_S)$ ($C_{TOT,MSB}$ is the total capacitance of higher bits CDAC), we have (4), where dw_i represents the digital bit weight of C_i. (4) indicates that dw of the capacitor under calibration equals to the sum of the dw of the capacitors which connect to V_{REF} after conversion minus the sum of the dw of the capacitors which connect to V_{REF} during sampling. The same conclusion can be drawn for the capacitors in other calibration groups.

During normal conversion, the final digital output is the sum of the digital bit weights of those capacitors kept to V_{REF}.

B. P-N MISMATCH AND COMPARATOR OFFSET CONSIDERATION

In the calibration process mentioned above, the N-side DAC is not involved at all. Ideally, the summing node of N-side DAC needs to connect to ground during sampling and then the N-side DAC remains static. However, the mismatch between P-side and N-side DAC would cause a non-zero differential voltage right after the top plate switches turn off. This voltage must be eliminated before calibration because it does not result from the capacitor mismatch in P-side DAC.

Moreover, the comparator offset also degrades the calibration accuracy significantly. According to the behavior simulation, the comparator offset must be smaller than about half LSB (~38 μV) to make the calibration effective. Previous work requires the comparator offset to be cancelled before the calibration, which increases the design complexity[11].

In this prototype, an extra SAR logic controlling C_{8N} to C_{25N} in the N-side DAC is initiated right after the sampling is completed. This SAR logic is designed to make the DAC differential voltage on the summing nodes successively approximate to the comparator offset before the calibration starts. Fig. 6 illustrates the DAC waveforms during the calibration.

As shown in Fig. 6, the calibration is always effective as long as the difference between the P-N mismatch voltage and comparator offset is smaller than ±78 mV which is the largest cover range of C_{8N} to C_{25N}. This is believed to be large enough according to the circuit simulation results with Monte-Carlo model.

$$\begin{cases} Q_{X,samp} = -V_{REF}C_i - V_{Y,samp}C_C \\ Q_{Y,samp} = \left(V_{Y,samp} - V_{REF}\right)\sum_j C_{j,REF,samp,low} + V_{Y,samp}\left(C_{TOT,LSB} - \sum_j C_{j,REF,samp,low}\right) + V_{Y,samp}C_C \\ \qquad = V_{Y,samp}C_{TOT,LSB} - V_{REF}\sum_j C_{j,REF,samp,low} + V_{Y,samp}C_C \end{cases} \tag{1}$$

$$\begin{cases} Q_{X,conv} = -V_{REF}\sum_j C_{j,REF,conv,high} - V_{Y,conv}C_C \\ Q_{Y,conv} = \left(V_{Y,conv} - V_{REF}\right)\sum_j C_{j,REF,conv,low} + V_{Y,conv}\left(C_{TOT,LSB} - \sum_j C_{j,REF,conv,low}\right) + V_{Y,conv}C_C \\ \qquad = V_{Y,conv}C_{TOT,LSB} - V_{REF}\sum_j C_{j,REF,conv,low} + V_{Y,conv}C_C \end{cases} \tag{2}$$

$$C_i = \sum_j C_{j,REF,conv,high} + \frac{C_C}{C_{TOT,LSB}+C_C}\sum_j C_{j,REF,conv,low} - \frac{C_C}{C_{TOT,LSB}+C_C}\sum_j C_{j,REF,samp,low} \tag{3}$$

$$dw_i = \sum_j dw_{j,REF,conv,high} + \sum_j dw_{j,REF,conv,low} - \sum_j dw_{j,REF,samp,low} \tag{4}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

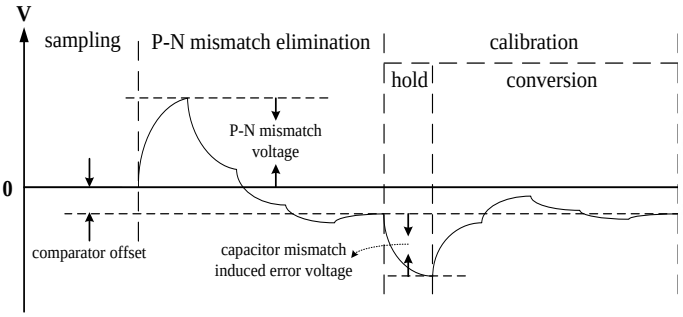


FIGURE 6. DAC waveforms illustration during a single calibration.

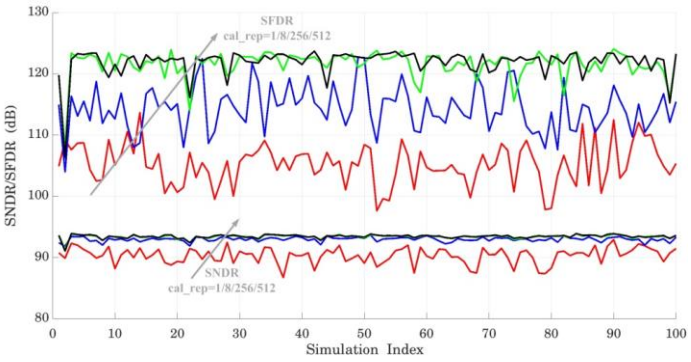


FIGURE 8. SNDR and SFDR with different calibration repetition times.

C. NOISE CONSIDERATION

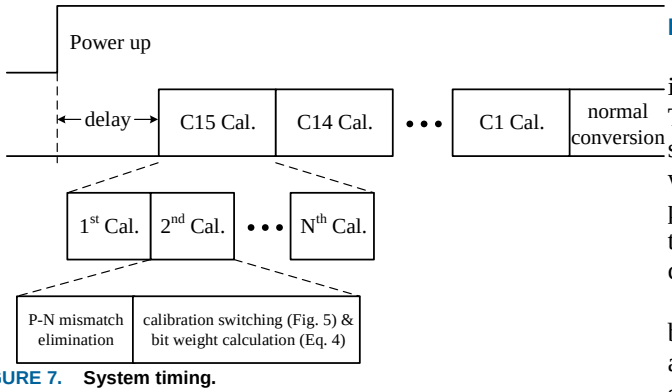


FIGURE 7. System timing.

As the calibration works in foreground, normally after power up, circuit noise would degrade the calibration accuracy. The calibration must repeat for multiple times and average the obtained digital bit weights. The complete system timing during calibration is shown in Fig. 7.

TABLE I
SYSTEM PARAMETERS FOR BEHAVIOR SIMULATION

Times of Monte-Carlo runs		100
Offset & Noise	Input-referred offset of comparator	10 mV_{RMS}
	Input-referred noise of comparator	15 μV_{RMS} (circuit simulation)
	V_{REF} noise	20 μV_{RMS} (circuit simulation)
	Sampling noise	13 μV_{RMS} (sampling capacitance is 24 pF)
Mismatch	Mismatch of unit capacitor (C)	1% RMS
	Mismatch of unit capacitor (C/8)	2% RMS
	Mismatch of C_C	5% RMS
	Calibration repetition times	1/8/256/512

Behavior simulation is done to verify the calibration technique. The system parameters used in the simulation are listed in Table I. Fig. 8 shows the SNDR and SFDR of 100 times Monte-Carlo simulations with different random capacitor mismatch data. It can be observed that the calibration needs to repeat for more than 500 times to completely average out the noise effect.

IV. DNL ENHANCEMENT

The digital calibration mentioned in the previous section is a post-processing activity operated in the digital domain. The final digital output is calculated as the accumulation sum of each bit weight. Even if the output code is closer to what is expected after the calibration, the code transition point is still decided by the original bit values. Therefore, the DNL result may not be perfect with digital bit weight calibration.

A DNL enhancement technique is proposed in this paper based on the following observation. To improve the accuracy of calibration, the fractional value capacitors, shown as C_{21P} to C_{25P} in Fig. 4, are involved in the SAR logic during the calibration. As a result, each bit weight is actually composed of integer part and fractional part, and so does the digital output during normal conversion. Limited by the ADC resolution, the fractional part in the digital output would be discarded eventually. The consequent effect should be cancelled out by a corresponding operation implemented in the analog domain. In other words, an analog value corresponding to the fractional part of the digital output needs to be subtracted by the switching of the fractional value capacitors.

The analog subtraction must satisfy the following three conditions:

a) It should be implemented somewhere before the conversion is completed, otherwise it is meaningless;

b) After the subtraction, the fractional part of the digital output should not change any more;

c) There should be some redundancy during the conversion thereafter.

To understand how the analog subtraction helps to improve the DNL, let's consider a simple example. Assume that the ideal values of the capacitors in the DAC are 8C, 4C, 2C, 2C, 1C, respectively, but their actual values are 8.5C, 4.25C, 2C, 2C, 1C and these bit weights are already known. The assumption is reasonable because after the self-calibration, which is proposed in Section III, is finished after power up, the exact bit weights of each capacitor are indeed known. The analog subtraction is designed to be implemented right after the third bit cycle, thus condition a) is satisfied. As the bit weights of the last two bits are actually integer numbers, condition b) is also met. Finally,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

the consecutive two 2C provides redundancy after the subtraction, thus condition c) is satisfied as well.

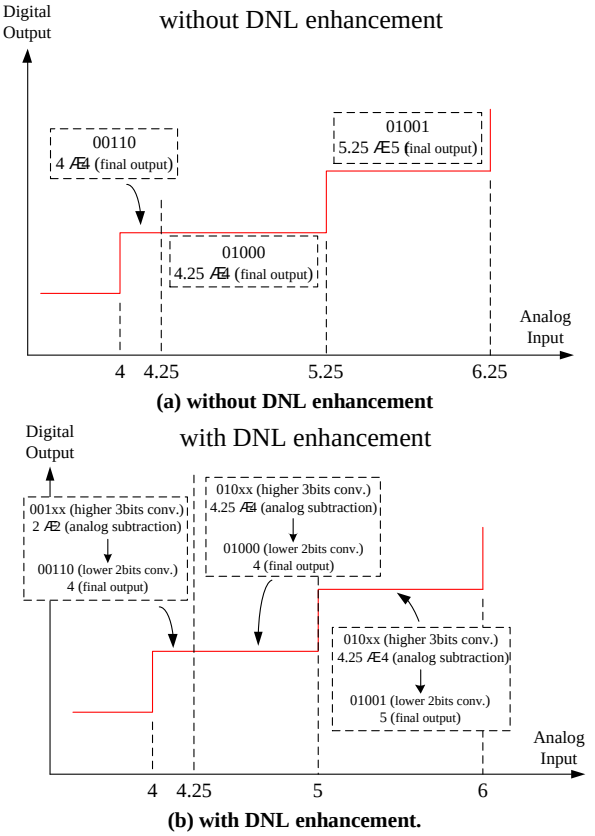


FIGURE 9. ADC transfer curve around code 5.

Some critical code transitions are analyzed in detail. Fig. 9 (a) shows part of the transfer curve without DNL enhancement. When the analog input is between 4 and 4.25, the original bit values are "00110", thus the accumulation result of the bit weights is 4, which is also the final digital output. When the input increases from 4.25 to 5.25, the original bit values become "01000", thus the accumulation result becomes 4.25. After the fractional part is discarded, the final digital output changes to 4. As the digital output remains the same when the input sweeps from 4 to 5.25, a DNL error of +0.25 LSB can be observed.

Fig. 9 (b) shows the same part of the transfer curve with DNL enhancement. For instance, when the input is between 4.25 and 5, the first three original bit values are "010", and the corresponding accumulation result of the bit weights is 4.25. At this moment, the switching of fractional value capacitors (not mentioned in this simple example) would subtract 0.25 from the DAC summing node voltage, making it decrease to 4 and then the succeeding bit cycles starts. After the conversion is done, the bit values are "01000" and the digital output is 4.

Going through the same process when the input is between 5 and 6, the result is depicted in Fig. 9 (b). As can be seen, because the fractional part is subtracted before the conversion is completed, all the transition points are now located at the integer numbers and the DNL error is eliminated. Another part of the transfer curve with and without DNL enhancement is shown in Fig. 10, which also demonstrates the effectiveness of this technique.

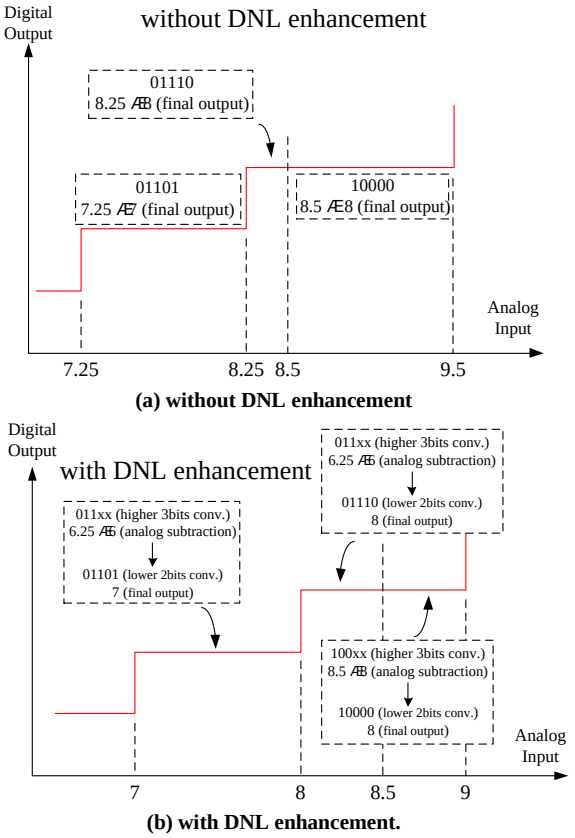


FIGURE 10. ADC transfer curve around code 8.

For the DAC designed in Fig. 4, the analog subtraction is designed right after the bit cycle of C_{18P}. The next bit capacitor C_{19P}, with the same value as C_{18P}, provides redundancy thereafter. As the capacitors C_{16P} to C_{20P} are not calibrated, their bit weights are integer numbers. Thus, the fractional part of the digital output would not change after the bit cycle of C_{18P}. The analog subtraction is implemented by switching the fractional value capacitors of N-side DAC from ground to reference, while those in P-side DAC remain static.

Although this technique is proposed to improve DNL, SNR is also benefited due to their relevance, which will be evident from the measurement results described in Section VI.

V. COMPARATOR DESIGN

The comparator is composed of a four-stage pre-amplifier and a clocked latch, as shown in Fig. 11. During the first 6-bit cycles, S_1 is on and S_2 is off. The output of the first stage pre-amplifier is directly fed to the latch, making the comparator work in high-speed mode. After that, S_1 is off and S_2 is on, making the comparator work in high-accuracy mode. In high-speed mode, the pre-amplifier takes

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

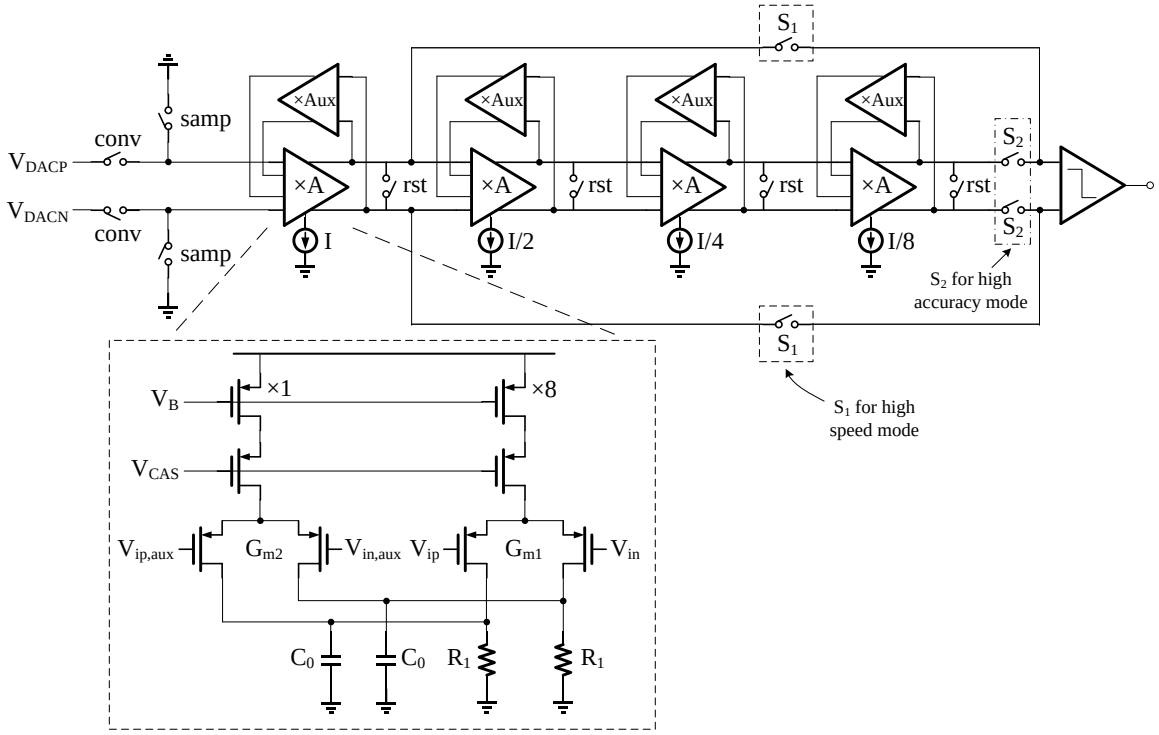


FIGURE 11. **The comparator simplified circuit.**

less time for settling, so the period of each bit cycle is made shorter than that in the high accuracy mode.

The total DC gain of the four-stage pre-amplifier is approximately ×1500. For attenuating the latch noise alone, a high DC gain of 1500 is not required. Actually, the high DC gain results from the multi-stage topology, which is used to reduce the noise of the amplifier itself, but not just the latch. The reason why the input-referred noise of a multi-stage amplifier is smaller than that of a single stage amplifier is explained in detail in the Appendix.

Considering that the input common mode of the comparator is close to 0 V, a PMOS input pair is used with resistor loads. The offset of each pre-amplifier is calibrated by an auxiliary input pair whose bias current is one eighth of the main input. The gain and bandwidth of each pre-amplifier are approximately the same but the bias current is reduced by half stage by stage. Reset signal of the pre-amplifier is generated from the DAC settling replica.

A. OFFSET CANCELLATION

Although the comparator offset does not affect the calibration (as mentioned in Section III) and the ADC linearity, the offset difference between the high-speed mode and high-accuracy mode must be small enough. Although the redundant bit is useful, there may not be enough headroom to correct other dynamic conversion errors if the redundant bit is used to cover the comparator offset mismatch. Moreover, the ADC offset error temperature drift is expected to be small. Therefore, the comparator offset cancellation is still essential in our design. For the pre-amplifier, input offset storage (IOS) and output offset storage (OOS) are two commonly used techniques to cancel the offset[12], but they both introduce extra capacitors in the signal path and thus affect the speed. In this design, the offset is calibrated based on an auxiliary G_m stage and cancelled through an extra input pair in the main amplifier. The basic idea is shown in Fig. 12[19].

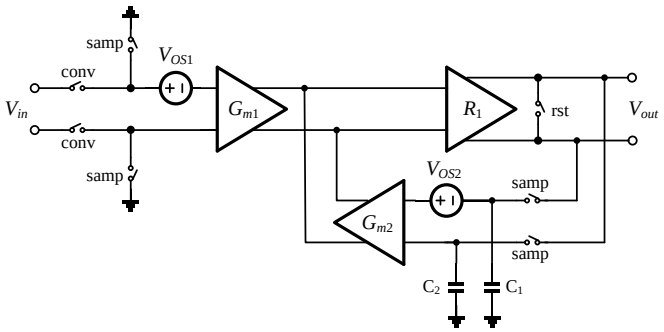


FIGURE 12. **Basic idea of the comparator offset cancellation.**

The input referred offset after calibration is reduced to:

$$V_{OS,tot} = \frac{V_{out}}{G_{m1}R_1} \approx \frac{V_{OS1}}{G_{m2}R_1} + \frac{V_{OS2}}{G_{m1}R_1} \quad (5)$$

For an input offset of several mV and a pre-amplifier gain less than 10, the residual input offset after calibration may be still larger than 1 mV.

An improved calibration scheme is shown in Fig. 13. An auxiliary amplifier is added in the auxiliary G_m stage to boost its equivalent transconductance. Meanwhile, the basic

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

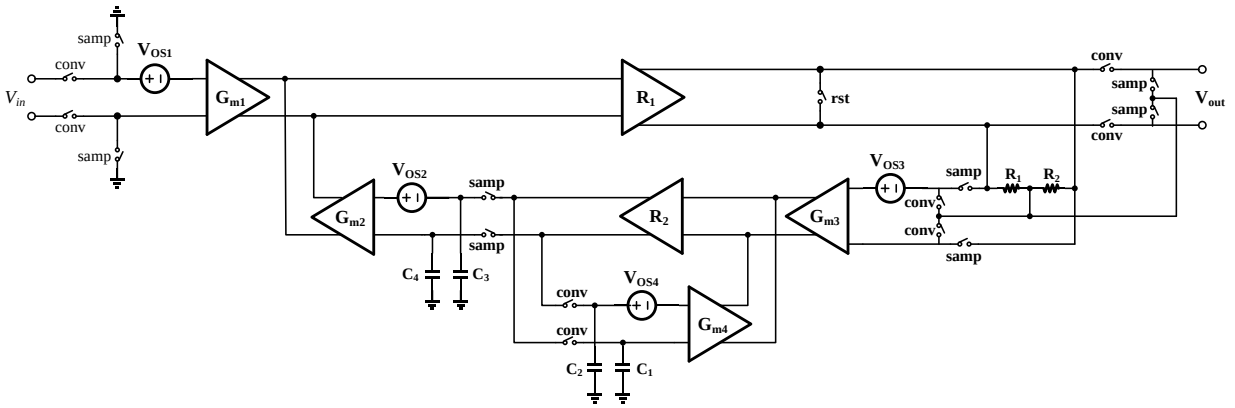


FIGURE 13. The offset calibration scheme using a gain-boosted auxiliary G_m stage.

calibration scheme is applied to the auxiliary amplifier and embedded in the calibration loop of the main amplifier. During conversion, the auxiliary amplifier works in calibration mode with its inputs short connected to the output common mode voltage of the main amplifier. During sampling, the main amplifier works in calibration mode.

By using the result from (5) and referring V_{OS2} to the input of G_{m3}, the equivalent input offset of the entire auxiliary G_m stage is now reduced to $V_{OS2}/G_{m3}R_2+V_{OS3}/G_{m4}R_2+V_{OS4}/G_{m3}R_2$. On the other hand, the equivalent transconductance of the entire auxiliary G_m stage is now boosted to $G_{m3}R_2G_{m2}$. With these results, (5) can be rewritten as (6) to express the residual input offset.

$$V_{OS,tot}=\frac{V_{OS1}}{G_{m3}R_2G_{m2}R_1}+\frac{V_{OS2}}{G_{m3}R_2G_{m1}R_1}+\frac{V_{OS3}}{G_{m4}R_2G_{m1}R_1}+\frac{V_{OS4}}{G_{m3}R_2G_{m1}R_1} \quad (6)$$

Because the auxiliary amplifier does not affect the speed of the main amplifier during ADC conversion, the auxiliary amplifier can be realized by a high gain folded-cascode structure with a gain of around 80 dB. Monte Carlo simulation indicates that the residual input offset of each pre-amplifier stage is now less than 20 μV.

The latch offset is minimized by the technique proposed in [13]. After the offset cancellation, the remaining offset difference between the high-speed mode and high-accuracy mode of the comparator can be covered by the redundancy right after the 6th bit cycle.

B. NOISE CONSIDERATION

Sampling noise, reference noise, and comparator noise are the three major noise contributions in this design. The sampling noise is decreased by choosing a large sampling capacitor (24 pF); while the reference noise can be suppressed by a large off-chip decouple capacitor (~10 μF) on the reference voltage. In this section, the pre-amplifier noise is analyzed in detail.

The noise current of the PMOS input pair ($4kT\gamma g_m$) and load resistor ($4kT/R_L$) both contribute to the output noise (the noise from the auxiliary input pair is ignored because it is much smaller than the main input). Considering that the output impedance is the parallel of R_L and C_L which is composed of C_0 and the gate capacitance of the next stage, the total output noise integrated over the entire frequency range is calculated as:

$$\overline{v_{n,out}^2}=\left(\gamma g_m R_L+1\right)\frac{kT}{C_L} \quad (7)$$

$\overline{v_{n,out}^2}$ can be referred to the input by dividing the square of gain, which is $A=g_mR_L$:

$$\overline{v_{n,in}^2}=\left(\frac{\gamma}{A}+\frac{1}{A^2}\right)\frac{kT}{C_L} \quad (8)$$

As can be observed, for a certain gain, the input referred noise is only a function of the load capacitor C_L, and thus an extra capacitor C_0 is used to reduce the noise while maintaining enough bandwidth for settling.

Another critical factor to decrease the noise is the multi-stage structure. Intuitively speaking, the output noise of the 1st stage is amplified by the follow-up three stages, but the magnification is attenuated at high frequency. On the other hand, suppose that the pre-amplifier is fast enough for the small signal to be fully settled, the output noise contribution from the 1st stage at the pre-amplifier output should be divided by the total *DC gain* of the pre-amplifier when referred to the input. Meanwhile, the noise contributions from the subsequent stages are negligible compared with that from the 1st stage. Therefore, the input-referred noise of a multi-stage amplifier is smaller than that of a single stage amplifier. Mathematical details are given in the Appendix.

The simulation shows that the input-referred noise of the four-stage pre-amplifier is less than 15 μV. The latch noise, referred to the input of latch, is about 1 mV which can be ignored as it is attenuated to 1 mV/1500 ≈ 0.7 μV when referred to the input of comparator. The overall noise breakdown of the ADC is shown as follows (V_{REF}=5 V):

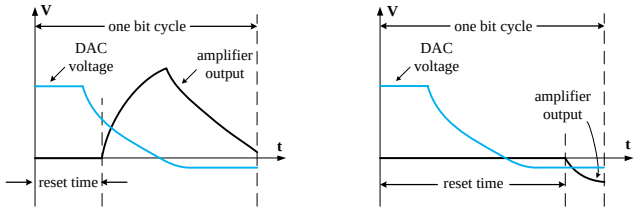
TABLE II
OVERALL NOISE BREAKDOWN

Quantization noise	Comparator noise	Reference noise	Sampling noise
$(22.0\ \mu V)^2$	$(14.8\ \mu V)^2$	$(20.9\ \mu V)^2$	$(13.1\ \mu V)^2$
Total noise		SNR	
$(36.2\ \mu V)^2$		93.8 dB	

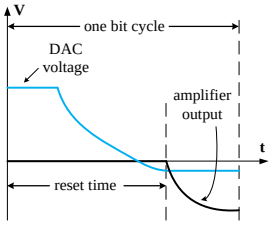
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

C. RESET TIMER

During the SAR bit cycle, the reset of the pre-amplifier is important to guarantee the comparator performance. As shown in Fig. 14(a), if the reset time is shorter than the DAC settling time, the output of the pre-amplifier may settle to a wrong direction at first and can barely return in the limited remaining time. In Fig. 14(b), the reset time is much longer than the DAC settling time. Under such situation, the input may not be fully amplified and thus the equivalent gain of the pre-amplifier significantly drops. The ideal case is shown in Fig. 14(c), where the reset time is just a little bit longer than the DAC settling time.



(a) Reset time shorter than DAC settling time. (b) Reset time longer than DAC settling time.



(c) Reset time equal to DAC settling time.

FIGURE 14. DAC voltage and pre-amplifier output.

To properly set the reset time, a DAC settling replica is designed, as shown in Fig. 15. The capacitor, C_1, C_3, C_7, and the switch control circuits, are all the same with those in DAC. The discharge time of C_1, C_3 and C_7 determines the pre-amplifier reset time for the 1st to 2nd bit cycles, the 3rd to 6th bit cycles, and the 7th to the last bit cycles, respectively.

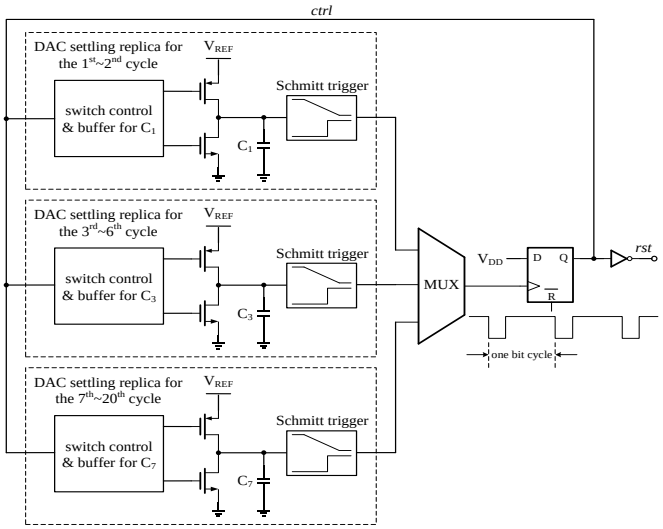


FIGURE 15. Comparator reset signal generation with DAC settling replica.

At the beginning of each bit cycle, the signal *ctrl* goes low, and then *rst* goes high, making the pre-amplifier start to reset. After the delay of the switch control and buffer, the capacitor starts to discharge, which is similar to the settling of DAC. The switch size is fine tuned so that the discharge time from V_{REF} to the threshold point of the Schmitt trigger is approximately equal to the DAC settling time. Once the Schmitt trigger flips, *ctrl* goes high again and then *rst* goes low, causing the pre-amplifier to start to work. The DAC settling time variation with process or temperature can be tracked by the circuit shown in Fig. 15.

VI. PROTOTYPE DESIGN AND MEASUREMENT RESULTS

The prototype ADC is fabricated in a 0.18μm 1P5M 5V CMOS process. Capacitors in the DAC are implemented by MIM (Metal-Insulator-Metal) capacitor. Both power supply and reference voltage are 5 V. The reference is provided externally by a high accuracy operation amplifier configured as a unity gain buffer with a 22-μF off-chip decoupling capacitor. The reference ground is separated from the circuit ground on chip.

The die microphotograph is shown in Fig. 16. The ADC core, including DAC, comparator, SAR logic, calibration logic, and RC oscillator, occupies an area of 1.7 mm × 3.3 mm. The RC oscillator provides the synchronous clock for SAR logic. The period of bit cycle during normal conversion is set to about 40 ns, leaving 200 ns for sampling. During the calibration, because the calibration time is of less importance, the period of bit cycle is set to about 160 ns so as to avoid any dynamic conversion errors affecting the calibration accuracy. The calibration repetition time for each capacitor is set to 1024 by default.

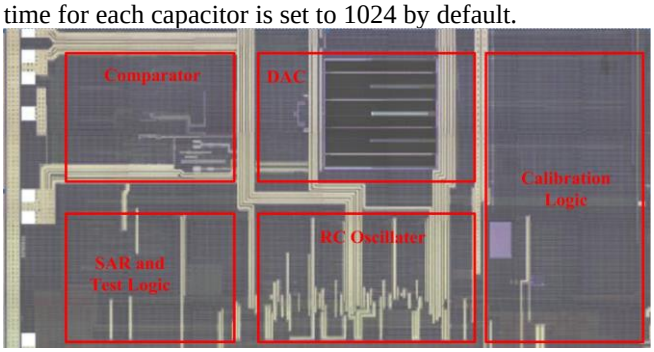
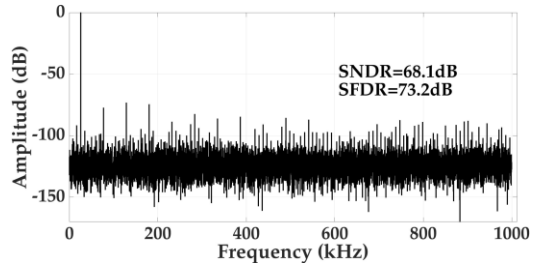


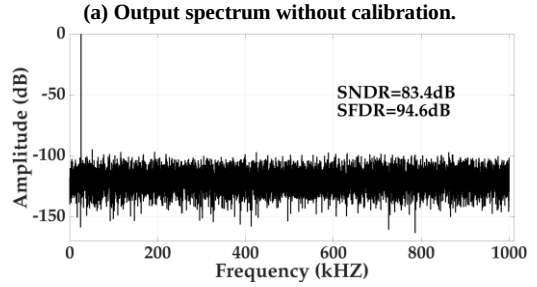
FIGURE 16. The die microphotograph.

Fig. 17 shows the output spectrum for the ADC operating at 1 MS/s with a 10-kHz input tone. Without calibration, lots of large spurs can be observed on the FFT plot. With calibration turned on but DNL enhancement turned off, the SNDR and SFDR are 83.4 dB and 94.6 dB, respectively. With both calibration and DNL enhancement technique, the SNDR and SFDR are further improved by 8.9 dB and 13.3 dB, respectively, and a 15.0-bit ENOB is achieved.

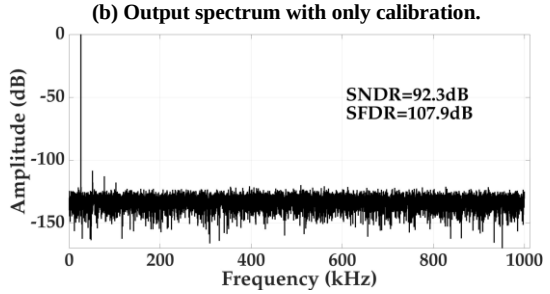
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access



(a) Output spectrum without calibration.



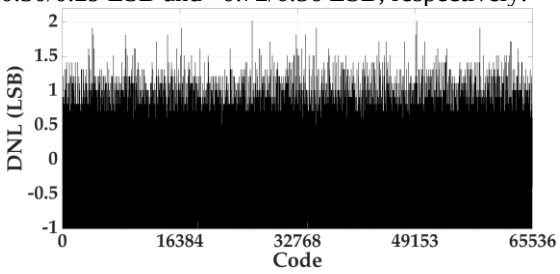
(b) Output spectrum with only calibration.



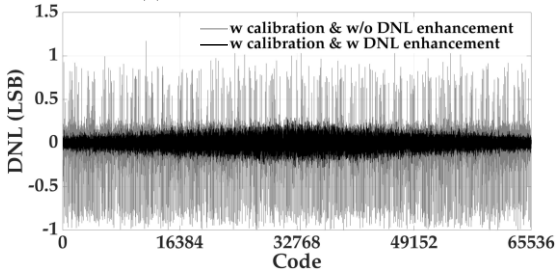
(c) Output spectrum with both calibration and DNL enhancement.

FIGURE 17. The ADC output spectrum at 10 kHz input tone.

The DNL and INL test results are exhibited in Fig. 18 and Fig. 19. Before calibration, lots of missing codes can be observed and the INL is several tens of LSB. After calibration, the DNL and INL are –1.00/1.17 LSB and –3.28/3.62 LSB, respectively. With both calibration and DNL enhancement, the DNL and INL are further reduced to –0.30/0.29 LSB and –0.72/0.56 LSB, respectively.

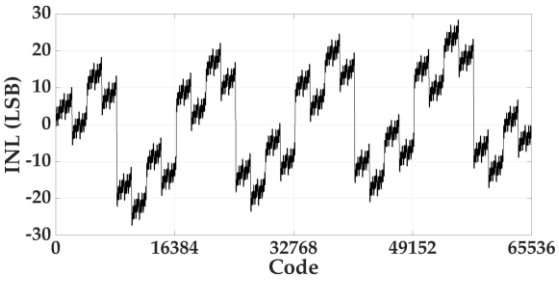


(a) DNL result before calibration.

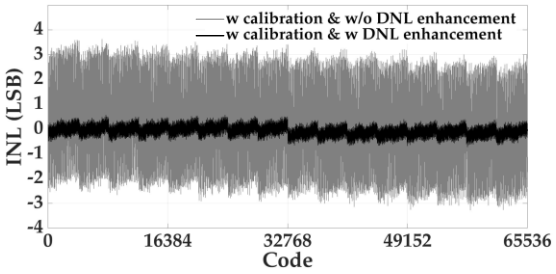


(b) DNL result after calibration w and w/o DNL enhancement.

FIGURE 18. The DNL results.



(a) INL result before calibration.



(b) INL result after calibration w and w/o DNL enhancement.

FIGURE 19. The INL results.

The SNDR and SFDR versus input frequency are shown in Fig. 20. The dynamic performance starts to degrade at several tens of kHz input, mainly because the large sampling capacitor (~20 pF) limits the sampling linearity at high frequency.

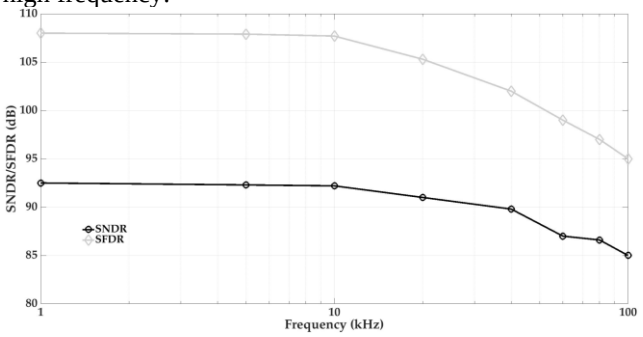


FIGURE 20. The SNDR and SFDR vs. input frequency.

A total of 360 chips from different manufacturing lots are tested and their INL results are summarized as shown in Fig. 21 (only the maximum of absolute value are counted). The INLs of about 63% chips are between 0.7~0.8 LSB. Most of the remaining chips show INL of 0.6~0.7 LSB (16%) or 0.8~0.9 LSB (22%). These results demonstrate a high yield of this chip in massive production.

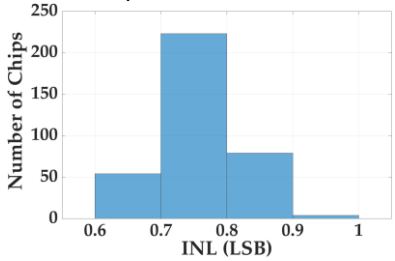


FIGURE 21. The INL statistical results of 360 chips.

The analog power consumed by the DAC and comparator is 25.8 mW, while the digital power consumption drawn by SAR logic, calibration logic, and

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

RC oscillator is 14.2 mW. The total power, consumed from the 5-V supply, is 40.0 mW. The figure-of-merit (FoM), defined as (SNDR+10log(BW/power)), is 166.3 dB. Table III shows the comparison with the state-of-the-art high-resolution ADCs.

VII. CONCLUSION

A 16-bit 1 MS/s pseudo-differential SAR ADC is presented in this paper. A differential DAC, with both monotonic and traditional switching, is designed to sample and convert the pseudo-differential input, providing the ADC with the same common mode rejection capability as fully differential circuit. The bit weights errors are fixed by a digital self-calibration technique which utilizes some of the LSBs capacitors to measure and calculate the bit weights of other capacitors. As the digital bit weight calibration along is not able to improve the DNL/INL performance, a DNL enhancement technique is proposed. It uses the fractional value capacitors to subtract an analog voltage from the DAC corresponding to the fractional part of the digital output. The digital calibration together with the DNL enhancement effectively improves both the dynamic and static performance of the ADC. The comparator is the most challenge circuit block in this ADC. An auxiliary G_m stage with gain boosting is used to calibrate the comparator offset to less than half LSB, while the comparator noise is minimized by component sizing and the multi-stage pre-amplifier topology. A prototype ADC fabricated in a 0.18-μm 5-V CMOS process achieves 15-bit ENOB, and the DNL and INL are within ±0.3 LSB and ±0.7 LSB respectively. The ADC draws 40 mW power from the 5-V supply and exhibits a 166.3 FoM.

TABLE III
SUMMARY AND COMPARISON WITH HIGH-RESOLUTION ADCS

	This work	[14]	[15]	[16]	[17]
Architecture	SAR	Cyclic	SAR	SAR	Pipe SAR
Process	0.18 μm	0.13 μm	55 nm	55 nm	0.18 μm
Resolution (bit)	16	16	16	16	18
Speed (MS/s)	1	0.5	1	16	5
SNDR (dB)	92.3	77.4	81	78	99
SFDR (dB)	107.9	N/A	N/A	98	100
DNL (LSB)	–0.3/0.3	–0.9/0.9	–0.3/0.3	–0.7/0.8	–0.4/0.4
INL (LSB)	–0.7/0.6	–6.1/6.1	–0.8/0.8	–1.9/2.3	–2/2
Power (mW)	40.0	6	7.0	16.3	30.5
VDD (V)	5	3	3.3/1.2	3.3/1.2	5/1.8
Calibration	On-chip	Cal. free	Off-chip	On-chip	Off-chip
FoM_S (dB)	166.3	153.6	159.6	165	179.3

APPENDIX

In this Appendix, the reason why the input-referred noise of a multi-stage amplifier is smaller than that of a single stage amplifier is explained in detail.

Suppose I_n^2 is the output noise current of each amplifier, and in our case $I_n^2 = 4kT\gamma g_m + 4kT/R$.

For a single stage amplifier, the total output noise voltage power integrated over the entire frequency range can be calculated as (R and C are the load resistance and capacitance respectively, f_0 is the -3dB bandwidth and f_0 =1/2πRC):

$$\overline{V_{n,out}^2} = \int I_n^2 \frac{R^2}{1+R^2C^2(2\pi f)^2} df = \int I_n^2 \frac{R^2}{1+\left(\frac{f}{f_0}\right)^2} df = I_n^2 R^2 \frac{\pi f_0}{2}$$

Divide it by the square of gain, we have the input-referred noise power of a single stage amplifier:

$$\overline{V_{n,in,1-stg}^2} = \frac{I_n^2 R^2 \pi f_0}{2A^2}$$

For a two-stage amplifier, both stages contribute to the total output noise while the noise of the 1st stage is amplified by the 2nd stage. The output noises power contributed from the two stages are:

$$\begin{cases} \overline{V_{n,out,1}^2} = \int I_n^2 \frac{R^2}{1+\left(\frac{f}{f_0}\right)^2} \frac{A^2}{1+\left(\frac{f}{f_0}\right)^2} df = \int \frac{I_n^2 R^2 A^2}{\left[1+\left(\frac{f}{f_0}\right)^2\right]^2} df = I_n^2 R^2 A^2 \frac{\pi f_0}{4} \\ \overline{V_{n,out,2}^2} = \int I_n^2 \frac{R^2}{1+\left(\frac{f}{f_0}\right)^2} df = I_n^2 R^2 \frac{\pi f_0}{2} \end{cases}$$

Adding the two terms above and dividing the sum by the square of total gain, we have the input-referred noise power of a two-stage amplifier:

$$\overline{V_{n,in,2-stg}^2} = \frac{1}{A^4}\left(\overline{V_{n,out,1}^2} + \overline{V_{n,out,2}^2}\right) = \overline{V_{n,in,1-stg}^2}\left(\frac{1}{2} + \frac{1}{A^2}\right)$$

In our case, A≈6.2, and thus the input referred noise power of a two-stage amplifier almost halves compared to that of a single-stage amplifier. Intuitively speaking, the output noise of the 1st stage is amplified by the 2nd stage, but the magnification is attenuated with frequency. On the other hand, when the noise contribution from the 1st stage is referred to the input, it is divided by the *DC* gain. Therefore, the noise contribution from the 1st stage to the input is smaller than the input-referred noise of a single stage amplifier. Meanwhile, the noise contribution from the 2nd stage is actually negligible compared to that from the 1st stage.

For a three-stage amplifier, the output noises power contributed from each of the three stages are:

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

$$\begin{cases} \overline{V_{n,out,1}^2} = \int I_n^2 \dfrac{R^2}{1+\left(\dfrac{f}{f_0}\right)^2} \dfrac{A^2}{1+\left(\dfrac{f}{f_0}\right)^2} \dfrac{A^2}{1+\left(\dfrac{f}{f_0}\right)^2} df = \int \dfrac{I_n^2 R^2 A^4}{\left[1+\left(\dfrac{f}{f_0}\right)^2\right]^3} df = I_n^2 R^2 A^4 \dfrac{3\pi f_0}{16} \\ \overline{V_{n,out,2}^2} = \int I_n^2 \dfrac{R^2}{1+\left(\dfrac{f}{f_0}\right)^2} \dfrac{A^2}{1+\left(\dfrac{f}{f_0}\right)^2} df = \int \dfrac{I_n^2 R^2 A^2}{\left[1+\left(\dfrac{f}{f_0}\right)^2\right]^2} df = I_n^2 R^2 A^2 \dfrac{\pi f_0}{4} \\ \overline{V_{n,out,3}^2} = \int I_n^2 \dfrac{R^2}{1+\left(\dfrac{f}{f_0}\right)^2} df = I_n^2 R^2 \dfrac{\pi f_0}{2} \end{cases}$$

Adding the three terms above and dividing the sum by the square of total gain, we have the input-referred noise power of a three-stage amplifier:

$$\overline{V_{n,in,3-stg}^2} = \frac{1}{A^6}\left(\overline{V_{n,out,1}^2} + \overline{V_{n,out,2}^2} + \overline{V_{n,out,3}^2}\right) = \overline{V_{n,in,1-stg}^2}\left(\frac{3}{8} + \frac{1}{2A^2} + \frac{1}{A^4}\right)$$

Now the input-referred noise power is only about 37.5% of that of a single stage amplifier.

Similarly, for a four-stage amplifier, the output noises power contributed from each of the four stages are:

$$\begin{cases} \overline{V_{n,out,1}^2} = I_n^2 R^2 A^6 \int \dfrac{1}{\left[1+\left(\dfrac{f}{f_0}\right)^2\right]^4} df = I_n^2 R^2 A^6 \dfrac{5\pi f_0}{32} \\ \overline{V_{n,out,2}^2} = I_n^2 R^2 A^4 \int \dfrac{1}{\left[1+\left(\dfrac{f}{f_0}\right)^2\right]^3} df = I_n^2 R^2 A^4 \dfrac{3\pi f_0}{16} \\ \overline{V_{n,out,3}^2} = I_n^2 R^2 A^2 \int \dfrac{1}{\left[1+\left(\dfrac{f}{f_0}\right)^2\right]^2} df = I_n^2 R^2 A^2 \dfrac{\pi f_0}{4} \\ \overline{V_{n,out,4}^2} = I_n^2 R^2 \int \dfrac{1}{1+\left(\dfrac{f}{f_0}\right)^2} df = I_n^2 R^2 \dfrac{\pi f_0}{2} \end{cases}$$

Adding the four terms above and dividing the sum by the square of total gain, we have the input-referred noise power of a four-stage amplifier:

$$\begin{aligned} \overline{V_{n,in,4-stg}^2} &= \frac{1}{A^8}\left(\overline{V_{n,out,1}^2} + \overline{V_{n,out,2}^2} + \overline{V_{n,out,3}^2} + \overline{V_{n,out,4}^2}\right) \\ &= \overline{V_{n,in,1-stg}^2}\left(\frac{5}{16} + \frac{3}{8A^2} + \frac{1}{2A^4} + \frac{1}{A^6}\right) \end{aligned}$$

Now the input-referred noise power is further reduced to about 31.3% of that of a single stage amplifier.

Calculation on a five-stage amplifier reveals that the input-referred noise power can be decreased to 27.3% of that of a single stage amplifier. The benefit compared to a four-stage amplifier is limited. As a tradeoff between noise and speed, we finally choose the four-stage topology. The power consumption is indeed increased when using multi-stage amplifier, but it is beneficial for a high SNR SAR ADC and the FoM of our chip is actually comparable to the state-of-the-art.

REFERENCES

[1] H. S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15 bit CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. 19, no. 6, pp. 813-819, Dec. 1984.

[2] Y. Kuramochi, A. Matsuzawa, and M. Kawabata, "A 0.05-mm^2 110-μW 10-b self-calibrating successive approximation ADC core in 0.18-μm CMOS," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC) Tech. Papers*, Nov. 2007, pp. 224-227.

[3] L. Du, N. Ning, J. Zhang, et al., "Self-calibrated SAR ADC based on split capacitor DAC without the use of fractional-value capacitor," *IEEJ Trans. Electrical and Electronic Engineering*, vol. 8, no. 4, pp. 408-414, 2013.

[4] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661-2672, Aug. 2011.

[5] H. Li, M. Maddox, M. C. W. Coln, et al., "A signal-independent background-calibrating 20b 1MS/S SAR ADC with 0.3ppm INL," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 242-243

[6] J. A. McNeill, K. Y. Chan, M. C. W. Coln, et al., "All-digital background calibration of a successive approximation ADC using the "split ADC" architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2355-2365, Apr. 2011.

[7] W. Liu, P. Huang, and Y. Chiu, "A 12-bit 50-MS/s 3.3-mW SAR ADC with background digital calibration," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2012, pp. 1-4.

[8] R. Xu, B. Liu, and J. Yuan, "Digitally calibrated 768-kS/s 10-b minimum-size SAR ADC array with dithering," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2129-2140, Jun. 2012.

[9] G. Wang, F. Kacani, and Y. Chiu, "IRD Digital Background Calibration of SAR ADC With Coarse Reference ADC Acceleration," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 1, pp. 11–15, Jan. 2014.

[10] Ying-Zu Lin, Chun-Cheng Liu, Guan-Ying Huang, et al., "A 9-Bit 150-MS/s subrange ADC based on SAR architecture in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 60, no. 3, pp. 570-581, Feb. 2013.

[11] M. Yoshioka, K. Ishikawa, and T. Takayama et al., "A 10-b 50-MS/s 820-μW SAR ADC With On-Chip Digital Calibration," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 410–416, Dec. 2010.

[12] B. Razavi, and B.A. Wooley, "Design techniques for high-speed, high-resolution comparators," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1916-1926, Dec. 1992.

[13] J. Hu, N. Dolev, and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Source Follower Residue Amplification," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1057-1066, Apr. 2009.

[14] H.-C. Choi, S.-B. You, and H.-Y. Lee et al., "A Calibration-Free 3V 16b 500kS/s 6mW 0.5mm^2 ADC with 0.13μm CMOS," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2004, pp. 76–77.

[15] M. Maddox, B. Chen, M. Coln, et al., "A 16 bit linear passive-charge-sharing SAR ADC in 55 nm CMOS," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC) Tech. Papers*, Nov. 2016, pp. 153–156.

[16] J. Shen, A. Shikata, L. D. Fernando, et al., "A 16-bit 16-MS/s SAR ADC With On-Chip Calibration in 55-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1149-1160, Apr. 2018.

[17] A. Bannon, C. P. Hurrell, D. Hummerston, and C. Lyden, "An 18 b 5 MS/s SAR ADC with 100.2 dB dynamic range," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 33–34.

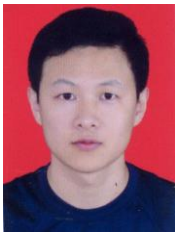
[18] Y.-H. Hwang and D.-K. Jeong, "Ultra-low-voltage low-power dynamic comparator with forward body bias scheme for SAR ADC," Electronics Letters, vol. 54, no. 24, pp. 1370-1372, Nov. 2018.

[19] B.Ravavi, "Precision Techniques," in *Principles of Data Conversion System Design*, Wiley-IEEE Press, 1995.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2019.2937384, IEEE Access

Panpan Zhang received the B.S. degree in microelectronics from Chongqing University of Posts and Telecommunications, Chongqing, China, in 2013, and the M.S. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2016. She is currently pursuing Ph.D. degree in Microelectronics and Communication Engineering from Chongqing University, Chongqing, China. Her research interests include the design of high-resolution analog-to-digital converters (ADCs), digital control techniques of switch mode power supply with applications to microprocessor voltage regulation modules and portable electronics.

Wenjiang Feng received the Ph.D. degree in electrical engineering from Chongqing University, Chongqing, China, in 2000. He is currently a Professor with the College of Microelectronics and Communication Engineering, Chongqing University. His research interests include all aspects of MIMO communication including limited feedback techniques, antenna design, interference management and full-duplex communication, cognitive radio, special mobile communication system, and emergency communication.



Peng Zhao received the B.S. degree in electronic science and technology from Harbin University of Science and Technology, Harbin, China, in 2004. He is currently a majordomo of technical in Shenzhen State Micro Electronics Co.,Ltd. His research interests include data converter design, switch mode power supply, power controller and regulators.

Xiaoping Chen received the B.S. degree and the M.S. degree in microelectronics and solidstate electronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2007 and 2010 respectively. He is currently a technical manager in Shenzhen State Micro Electronics Co.,Ltd. His research interests include successive-approximation register (SAR) analog-to-digital converter (ADC) design, digital control for dc–dc converters and power electronic systems.

Zongjiang Zhang received the B.S. degree and the M.S. degree in microelectronics and solidstate electronics from Guizhou University, Guiyang, China, in 2008 and 2011 respectively. He is currently a project manager in Shenzhen State Micro Electronics Co.,Ltd. His research interests include successive-approximation register (SAR) analog-to-digital converter (ADC) design, digital control of power converters, modeling and control techniques, mixed-signal IC design.