A Multi-Standard 1.5 to 10 Gb/s Latch-Based 3-Tap DFE Receiver With a SSC Tolerant CDR for Serial Backplane Communication

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Abstract—This paper presents a 1.5 to 10 Gb/s SATA/SAS/FC receiver in 65 nm CMOS. The multiple constraints set by industry standards ask for a receiver architecture capable of simultaneously addressing channel loss impairments, high frequency-difference tracking and low serial to parallel latency.

An adaptive 3-tap DFE data recovery is based on a direct-feedback topology to provide a continuous equalized signal assuring a robust clock-data self-alignment. A latch-based DFE topology has been developed to overcome the classical DFE feedback loop-delay issue. A digital early-late clock recovery has been proven for ±5000 ppm SSC tracking. Extensive digital features allow self-calibration and internal eye analysis.

The device, realized in a 65 nm technology, supports more than 36° FR4 at 6 Gb/s with SSC and 28° at 8.5 Gb/s while keeping 0.4 UI of additional sinusoidal jitter tolerance, consuming 140 mW from 1 V.

Index Terms—Adaptive equalizers, clock and data recovery, current-mode logic, data communication, decision feedback equalizers.

I. INTRODUCTION

ulti-gigabit per second serial transceivers are fast replacing older parallel interfaces in many applications. The industry standards for hard disk drives interconnection represent an example of this trend, showing a migration from parallel advanced technology attachment (PATA) to serial advanced technology attachment (SATA) and from small computer system interface (SCSI) to parallel advanced technology attachment (PATA) to serial advanced technology attachment (SATA) to serial attached SCSI (SAS).

The demand for high speed serial interconnections operating through high-loss (>20 dB Nyquist) cables and backplanes explains the recent research effort in the area of equalization techniques in order to tackle typical impairments, mainly intersymbol interference (ISI) and cross-talk.


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“Feed-forward” equalization (FFE) by transmitter pre-emphasis [1] or receiver equalization [2] has resulted in an effective technique to obtain wider eye opening at the receiver samplers in the presence of ISI. These techniques apply a controlled high pass shaping of the data, thus reversing the low-pass behaviour of the channel. With the increase of the channel losses and in the presence of cross-talk interference, decision feedback equalization (DFE) has become a widely diffused technique, even in conjunction with receiver or transmitter FFE [3]–[6]. By subtracting the ISI of the previous bits from the one under detection, DFE results in higher rejection of noise and crosstalk with respect to equalization schemes based on FFE only [7].

In this scenario, industry needs towards a multi-standard receiver addressing 1.5-3-6 Gb/s SATA/SAS and 2.125-4.25-8.5 Gb/s Fiber Channel (FC) are motivated by cost reasons as it would serve the main emerging data storage applications. On the other hand, different standards entail different challenges.

The extension of FC to an 8.5 Gb/s backplane interconnection calls for the above mentioned enhanced equalization techniques in an environment traditionally characterized by other constraints like serial to parallel data latency and fast locking time for phase jumps recovery (<2500 Unit Intervals—UI), but with a limited frequency difference between the transmitter and receiver reference clocks (±200 ppm). At the same time, with the increase of the data rate to 6 Gb/s, advanced data equalization is now a requirement also in the SATA/SAS environment, where traditionally one of the main challenge of the receiver has been “spread spectrum clock” (SSC) tracking. To minimize the electromagnetic interference the transmitted data is modulated in frequency by a triangular shape causing a frequency drift between 0 and ±5000 ppm (SATA down-spreading) or between ±2500 ppm (SAS center spreading) [8]. This asks the receiver to be able to track this large amount of frequency drift with the additional challenge of its time-variable triangular profile.

The development of a receiver architecture capable to withstand the eye closure jointly caused by channel impairments and SSC stress is the aim of this work [9]. The receiver employs a digital early-late clock and data recovery (CDR) tailored to SSC tracking. The joint operation between CDR and equalization has been optimized by the use of a direct-feedback DFE and a latch-based topology has been developed to overcome the classical DFE feedback delay issue. Ad hoc techniques have been applied to satisfy multi-standard and latency requirements from the SATA/SAS/FC standards.
The paper is organized as follows. Section II describes the receiver architecture. Section III covers the analog data recovery and DFE implementation. Section IV presents the CDR. Section V details the measured performances and Section VI concludes the paper.

II. ARCHITECTURE

This section analyzes the key choices behind the DFE topology selection and presents the adopted multi-standard receiver architecture.

A. Direct Feedback vs Loop Unrolling DFE

The DFE topology selection must take into account both data and clock recovery constraints. Two main topologies have been widely used in high speed serial links: direct feedback and loop unrolling, as shown in Fig. 1 assuming a 1-tap example.

The primary challenge of direct feedback in data recovery consists in feeding back the decision in less than 1 UI [Fig. 1(a)]. Due to speed concerns, most multi Gb/s DFEs employ loop unrolling techniques [10], [11], relaxing the first tap feedback. The data is split into two parallel paths precomputing the two possible values corresponding to positive and negative corrections. When the former bit is finally decided, the multiplexer selects the correct value [Fig. 1(b)].

On the other hand, the implementation of transition-based early-late CDRs [12] requires the data to be sampled both in the middle of the eye and at the edge, forcing additional constraints to the DFE architecture. By splitting the data between different paths, loop unrolling does not provide a continuous equalized signal to the CDR. As shown in Fig. 2 for 1-bit ISI, when a transition follows consecutive bits (“low rate patterns”—e.g. 110), the two bits defining the transition will be shifted by the same ISI amount. In this case, edge samplers can be added to the same nodes (b, c) of the data samplers of Fig. 1(b). On the contrary, when a transition follows alternating bits (“clock patterns”—e.g. 110), the two bits defining the transition will be shifted by opposite amounts, thus requiring the edge samplers threshold at the average between the two data levels, namely 0 V.

In addition to the above mentioned pattern-dependent edge threshold, a self aligned CDR would require also an additional edge sampling phase [CKE in Fig. 1(b)]. The simulation example in Fig. 3 shows the eye diagram at node (a) of Fig. 1(b). The eye opening available to a data sampler working when the previous detected bit is 1 is shown in gray. The sampling threshold has been raised to c1, as in path (b) of Fig. 1(b). It can be seen that the optimal sampling position can be obtained as a 1/2 UI shift from the phase φ1 resulting from the convergence of a CDR based on low rate patterns. On the contrary, a CDR based on clock patterns will converge to the transition phase φ2 resulting in delay. To compensate this effect, a phase shift should be added to the clock pattern edge detectors.

To avoid excessive loading in the critical signal path and in order to simplify the CDR architecture, solutions to the above mentioned issues consist in processing edge samples from non-DFE equalized data [3], [4] or in transition filtering [13]. Limiting CDR edge analysis to a subset of data sequences can result in sub-optimal operation with data patterns not including these sequences. For this reason, to implement a robust clock-data self-alignment, a direct feedback DFE topology has been selected, developing a latch-based architecture in order to minimize the feedback delay.

B. Receiver Architecture

The receiver architecture is shown in Fig. 4. A programmable gain amplifier (PGA) is followed by a linear feed forward equalizer (FFE) whose purpose is to complement the following DFE equalization which is intrinsically limited within a finite time span. Three parallel paths sample the incoming data stream and convert it to a lower bit rate by means of demultiplexers. The center path (C) implements a three-taps direct feedback DFE. The DFE is shared with the top path (E), dedicated to CDR edge sampling, and with the bottom auxiliary path (A), dedicated to DFE adaptation.

A digital CDR core receives demuxed C and E samples and drives three phase interpolators synthesizing the C, E and A
To address the FC requirement of a base-10 word alignment with minimal latency, the C-path demux has an additional 10-bits output to feed the data recovery word-aligner (WA). An overall serial to parallel latency lower than 40 UI is assured.

A DFE adaptation core based on a least mean squares (LMS) algorithm is fed by the same WA demux and by the auxiliary 10-bits demux of path A which includes threshold-programmable (Σ) samplers. The LMS performs real-time offset correction of the input linear chain and automatic threshold adaptation of the A samplers together with the DFE taps.

After DFE convergence, a real-time eye opening monitor (EOM) is implemented by controlling the sampling phase and thresholds of the A path. Comparing the samples of the A and C path, the internal eye opening at the samplers input is detected (Fig. 5). The EOM is also employed during the receiver start-up to automatically adapt the PGA and FFE to data amplitude and channel loss.

III. DATA RECOVERY DESIGN

A. Programmable Gain Amplifier and Linear Equalizer

The PGA allows the linear operation of the DFE input chain, regulating the internal data swing to about 0.6 Vppd from an input swing between 0.4 V and 1.6 Vppd.

The circuit diagram is shown in Fig. 6. The received signal is split in two coarse gain paths by a resistive divider in the input matching network. The selected data path is chosen by enabling one of the two current-mode logic (CML) stages. A fine gain tuning is set by changing the resistive source degeneration of the differential pairs. Programmable currents injected in the termination network allow offset compensation of the input linear chain.

The FFE circuit, depicted in Fig. 7, consists of three CML stages, each providing four equalization steps between 0 dB and 4 dB at the Nyquist frequency. Each stage can be programmed varying both the capacitance and the degenerating resistance,
allowing the optimization of the dynamic range at the DFE input for a given equalizer boost.

B. 3-Taps Direct Feedback DFE

A conventional direct feedback DFE based on half-rate clocking is reported in Fig. 8(a). The DFE correction node (a) adds data and feedback currents and feeds decision flip-flops. Multiplexers are inserted in the feedback path due to half-rate operation.

In order to minimize feedback delay, the implemented solution feeds the first tap from the output of the first latch, as shown in Fig. 8(b). To maximize the mux sensitivity, an additional CML gain stage (C) has been added at the mux input. The time diagram is shown in Fig. 9. By selecting the latch switching to the hold state, the mux incorporates the function of the second latch in a sampling FF. At the selection time, due to the evaluation state of the latch, the mux finds its input already available. This causes the propagation delay to be limited to the mux delay, hence avoiding the regeneration time of an additional latch. Simulation results have shown a 40% delay reduction versus the implementation of Fig. 8(a).

The DFE correction has been designed in CML logic (Fig. 10). Shunt peaking has been used for bandwidth extension. Small inductors have been implemented with the differential spiral topology shown in a two-metal example in Fig. 11. With this topology a 2 nH differential inductor in six metal layers requires a core area of $20 \times 20 \, \mu m^2$. The self-resonance of the inductor is higher than 20 GHz.

The sampling latch has been designed with the pseudo-CML topology of Fig. 12. A CML logic for the data inputs allows maximizing latch sensitivity while full swing CMOS levels have been used to minimize power consumption versus a CML clock.
distribution. Due to its pseudo-differential topology the proposed latch allows operation with a low-voltage power supply, while assuring the low setup and hold times of a CML solution.

C. DFE Adaptation

DFE adaptation is performed by a sign-error least mean square (LMS) algorithm [14]. The algorithm requires measuring the sign of the error \( e \) between the equalized and the expected eye height. For this purpose, the programmable thresholds \( (\text{TH}^+ / \text{TH}^-) \) in Fig. 4 of the auxiliary samplers are set to the expected positive and negative eye height.

The sign of the error \( e(i) \) caused by the ISI on the bit \( a(i) \) is directly provided by the auxiliary samplers and correlated with the previous bit \( a(i-n) \) through the product \( \text{sign}(e(i)) \cdot a(i-n) \).

The result is then integrated to update the DFE tap \( c_n(i) \) according to the LMS iterative procedure:

\[
c_n(i) = c_n(i-1) + u \cdot \text{sign}(e(i)) \cdot a(i-n).
\]  

(1)

The resulting \( c_n \) is rounded to integer values to be applied to the DFE adder.

In a similar way, the offset of the input linear chain (offset) is compensated in the PGA by means of the following iteration:

\[
\text{off}(i) = \text{off}(i-1) + u \cdot \text{sign}(e(i)).
\]  

(2)

The integration constant \( u \) controls the rate of the LMS adaptation and the steady state variance of the DFE and offset taps.

To minimize the load on the DFE node, only two auxiliary samplers are used, placing the positive and negative thresholds \( \text{TH}^+, \text{TH}^- \) on the sampler driven by the rising and falling edge of the clock, respectively. This requires performing the above LMS iterations only when positive bits are detected on the rising edge of the clock \([a(i)=2k=1]\) and negative bits on the falling edge \([a(i)=2k+1=-1]\).

The calculation of \( c_0 \) from (1) is used to adapt the threshold \( \text{TH} \).

IV. CLOCK RECOVERY DESIGN

A. CDR System Analysis

The CDR implements a classical bang-bang early-late technique consisting in detecting a clock early or late event from the comparisons of two data samples, in the center (C) and in the edge (E), when a data transition occurs [12]. The core of the CDR is the proportional-integrative (PI) controller of Fig. 13(a). \( N_{\text{chmx}} \) demuxed samples from the data center and edge enter a XOR matrix to identify early-late events, whose number is counted and multiplied by a proportional gain \( K_P \). The result increments an integer cyclic accumulator and when the accumulator cycle \( C \) is reached the phase is advanced or delayed by one step, depending on the occurrence of overflow or underflow.

The drawback of the above mentioned proportional controller is its limited capability in frequency drift tracking. In the presence of a constant phase shift, the number of UIs \( (N_{\text{UIP}}) \) required to reach an accumulator cycle \( C \) can be calculated from the relation

\[
N_{\text{UIP}} \cdot T_d \cdot K_P = C
\]  

(3)

where \( T_d \) is the transition density of the incoming data.

From the ratio between the phase update \( (1/N_{\text{PH}} = N_{\text{PH}} \)

being the number of phases in one UI) and the required number of UIs \( N_{\text{UIP}} \), the maximum Proportional Tracking (ppm) results in

\[
\text{Pt}_{\text{ppm}} = \frac{T_d \cdot K_P}{C \cdot N_{\text{PH}}} \cdot 1e6
\]  

(4)

Increasing \( K_P \) to satisfy frequency drift requirements leads to increasing loop bandwidth and, in the end, jitter [15]. For this reason an integrative path is added, which allows to track a constant frequency drift without requiring a continuous update from the proportional path.

The same analysis leading to (4) can be done for the integrative path. Assuming the cyclic accumulator is updated any \( N_{\text{chmx}} \) UIs, the following relation results:

\[
N_{\text{UII}}/N_{\text{chmx}} \cdot t_{\text{max}} = C
\]  

(5)

where \( N_{\text{UII}} \) is the number of UIs required by a full-scale value \( (t_{\text{max}}) \) of the integrative path to cause a cycle slip. From (5), the maximum Integrative Tracking (ppm) can be calculated, as done for (4), as the ratio between the phase update and the required number of UIs \( N_{\text{UII}} \):

\[
t_{\text{ppm}} = \frac{t_{\text{max}}}{C} \cdot \frac{1}{N_{\text{chmx}} \cdot N_{\text{PH}}} \cdot 1e6
\]  

(6)

Equation (6) shows that a constant frequency drift tracking is not a function of \( K_P \), thus relaxing the request of the loop bandwidth.

SSC tracking adds additional constraints. The SSC shows a triangular-shaped non-constant frequency drift, thus requiring a continuous update of the integrative accumulator. To gain insight, we can calculate the resolution \( (t_{\text{res}_{\text{ppm}}}) \) of the integrative path, defined as the frequency tracking increase caused by a unitary integrative increment:

\[
t_{\text{res}_{\text{ppm}}} = \frac{t_{\text{ppm}}}{t_{\text{max}}}
\]  

(7)

The number of UIs \( (N_{\text{UIR}}) \) causing this unitary integrative increment can be extracted from the identity:

\[
N_{\text{UIR}} \cdot T_d \cdot K_I/K_S = 1
\]  

(8)
Fig. 13. Proportional-integrative CDR. (a) Block diagram. (b) Loop gain.

Dividing $I_{\text{res}_{\text{ppm}}}$ by $N_{\text{ULT}}$, the maximum Integrative Slope Tracking (ppm/UI) results in the following:

$$I_{\text{st}_{\text{ppm/UI}}} = \frac{T_d \cdot K_I}{N_{\text{dmux}} \cdot N_{\text{FH}} \cdot C \cdot K_S} \cdot 10^6 \quad (9)$$

Equation (9) shows that SSC slope tracking will require maximizing the gain of the integrative path. On the other hand, a linear model of the loop gain results in a 40 dB/dec region defined by $K_I$ and in a 20 dB/dec region defined by $K_P$ [Fig. 13(b)]. Increasing $K_I$ reduces the phase margin of the system, thus also requiring an increase in $K_P$. Unfortunately, the overall latency of the digital loop will limit the allowable increase in $K_P$ and as a consequence in $K_I$, thus limiting the jitter tolerance performances during SSC tracking. This leads to the conclusion that latency minimization is the key factor to improve the slope tracking capability of the CDR.

B. CDR Implementation

The CDR architecture is shown in Fig. 14. To minimize loop latency the CDR is implemented in only three digital stages and it is always clocked at 750 MHZ in SSC tracking. This is done by means of multi-rate demuxes ($N_{\text{dmux}} = 2, 4, 8$ for 1.5, 3, 6 Gb/s). A ratio 12 is used in FC 8.5 Gb/s to limit the maximum CDR frequency. To assure adequate phase margin, $C$ and $I_{\text{ULR}}$ are not limited to binary values, allowing bandwidth optimization in each operation rate. Moreover, bandwidth variation with $T_d$ is minimized by counting the number of transitions in each demuxed word and correcting the proportional and integrative gains. To minimize complexity, the transition count is quantized and only 3 possible gain steps are employed (0.5, 1, 2).

The cyclic accumulator is implemented by a 10b unsigned adder. In case one of the two least significative bits changes its value, the phase is updated and the sign of the adder input is used as the phase update direction. The integrative accumulator consists of a saturating 15b signed adder, using the nine most significative bits ($K_S = 64$) as the integrative contribution. This results in both $C$ and $I_{\text{ULR}}$ being equal to 256, leading to $I_{\text{ppm}_{\text{lim}}} = \pm 3000$ ppm in 6 Gb/s operation with 32 phases per UI. A double phase step can be set to reach ±7800 ppm. To preserve the resolution $I_{\text{res}_{\text{ppm}}}$ in lower rate operation, the reduction of $N_{\text{dmux}}$ is compensated by a programmable decimator, periodically blanking the injection of the integrated value into the cyclic accumulator. For FC fast locking, CDR gains can be increased for a fixed time and then set back to nominal values, which are optimized for jitter tolerance.

C. DEMUX

The demux is implemented with the shift register topology of Fig. 15. To minimize area and power consumption the same shift register is shared between the CDR and the word-align (WA) by means of two independent parallel loads (L1, L2) at different rates. Due to the use of independent dividers, alignment between the two CDR de-multiplexers must be assured. The same applies to the two 10-bits de-multiplexers of the data recovery. Alignment between dividers is checked by a dedicated logic at every period of the divided clock. When a misalignment is detected,
one of the two dividing ratios is changed for a clock period to force a divider cycle slip.

D. Phase Interpolator

The CDR drives three phase interpolators synthesizing 32 phases ($\phi$) for UI. Two half-rate quadrature differential clocks phases are mixed by means of two weighting factors $X(\phi)$ and $Y(\phi)$, obtaining $Z(\phi) = Y(\phi) \cdot \sin(2\pi f t) + X(\phi) \cdot \cos(2\pi f t)$. where

$$\phi = \arctan\left[\frac{Y(\phi)}{X(\phi)}\right].$$

To keep positive weighting factors, the overall interpolation range of $2\pi$ is divided into four quadrants, each employing the appropriate polarity of the two clock phases to be interpolated.

The interpolator consists of four blocks, each made of identical differential pairs driven by the same clock phase. All the differential pairs drive the same load (Fig. 16). To preserve the output common mode, each phase $\phi$ is synthesized keeping constant the overall number of active cells inside the two blocks defining the selected quadrant. This leads to the additional relation:

$$Y(\phi) + X(\phi) = \text{const.}$$

A possible solution of (10) and (11) is

$$X(\phi) = \frac{\tan \phi}{1 + \tan \phi}, \quad Y(\phi) = \frac{1}{1 + \tan \phi}. \quad (12)$$

To have a good approximation of (12), minimizing the phase step variation within the $2\pi$ range, the number of elements that are switched to advance or delay the synthesized phase $\phi$ is non-uniformly set. 80 unitary elements of the overall 320 are simultaneously used, achieving a phase step precision better than 10%.

V. MEASURED RESULTS

The receiver has been implemented in a 65 nm CMOS technology from STMicroelectronics. Fig. 17 shows a chip micrograph. The core occupies 1 mm × 330 μm. The chip is fed by a full-rate differential clock that is internally divided to generate I/Q half-rate reference clocks. A serial data output is included to check the integrity of the recovered data before de-multiplexing while an internal parallel pseudo-random bit sequence (PRBS) checker allows verifying the whole deserializer path.

The dies have been wire-bonded in a plastic BGA package and plugged in a high frequency socket on a FR4 board with 2-inches differential input traces. The device has been tested at 1 V supply, consuming 140 mW at 8.5 Gb/s. A controlled frequency offset, either constant or SSC-modulated, has been applied to the reference clock. Various backplane lengths have been inserted between a pattern generator and the receiver data input.

During start-up, the receiver automatically calibrates the PGA and FFE to the incoming signal by means of the internal eye opening monitor. A serial interface allows the closing of the adaptation loop using a PC software, hence giving the flexibility of testing various adaptation algorithms. The DFE is self-adapted by the internal LMS. An example of the resulting internal eye opening for different channel lengths is shown in Fig. 18. After the adaptation, a variable amount of sinusoidal jitter is applied to the pattern generator to verify the jitter tolerance of the receiver.

Fig. 19 shows the sinusoidal jitter tolerance while receiving a PRBS7 pattern at 3 Gb/s with 5000 ppm SSC and at 4.25 Gb/s with a 200 ppm frequency difference. The receiver tolerates...
0.6 UI of sinusoidal jitter on top of the random jitter of the data and clock sources (~0.1 UI).

Increasing the operation frequency to 6 and 8.5 Gb/s allows the verification of the joint performance of equalization and clock recovery. The results are shown in Fig. 20. The device supports more than 36\% FR4 (22 dB loss) at 6 Gb/s with SSC and 28\% (24 dB loss) at 8.5 Gb/s while keeping 0.4 UI of additional sinusoidal jitter tolerance. Removing the channel loss allows evaluating the CDR performances, showing a sinusoidal jitter tolerance of 0.6 UI on top of the random jitter.

To complete the analysis, the equalization performances have been verified under a minimal frequency difference (50 ppm).

Fig. 18. 8.5 Gb/s internal eye opening.

Fig. 19. 3 Gb/s and 4.25 Gb/s sinusoidal jitter tolerance.

Fig. 20. 6 Gb/s and 8.5 Gb/s sinusoidal jitter tolerance.

Fig. 21. High frequency sinusoidal jitter tolerance vs channel loss.

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Fig. 19. 3 Gb/s and 4.25 Gb/s sinusoidal jitter tolerance.

Fig. 20. 6 Gb/s and 8.5 Gb/s sinusoidal jitter tolerance.

Fig. 21. High frequency sinusoidal jitter tolerance vs channel loss.

Table I gives a receiver summary.

VI. SUMMARY

This paper has presented a multi-standard SATA/SAS/FC receiver in 65 nm CMOS. A direct feedback 3-taps DFE topology,
complemented by a linear equalizer, has been used in conjunction with an early-late bang-bang CDR. The CDR has been tailored to SSC tracking and multi-standard operation. Design features such as half-rate clocking, latch-based DFE and integrated spiral inductors have been used to improve the high speed performances. Experimental results have shown the device capability to adapt to different channel lengths and operating speeds, hence satisfying the requirements of the addressed standards.

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REFERENCES


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In the same year he joined STMicroelectronics, Italy, working as an analog IC designer for power management and control. From 1998 to 2000, he led the analog design of the Wireline Division. In 2000, he started working on multi-gigabit CMOS and BiCMOS clock-data recoveries and PLLs for serial communication.

Mr. Pozzoni is presently leading the Radio Frequency and High Speed design group in the Studio di Microelettronica, a Scientific Laboratory in cooperation between STMicroelectronics and the University of Pavia. His research interests include multi-gigabit serial interfaces for I/O backplanes, millimetric-wave radio frequency design and frequency synthesis.

Simone Erba was born in Como, Italy, in 1976. He received the Laurea degree in electronics engineering from University of Pavia, Italy, in 1999.

From 2001 to 2002, he held a grant from STMicroelectronics in Pavia, working in RF analog design for radio communications. In 2002 he joined STMicroelectronics as an analog designer for telecommunication/datacom high speed serial interfaces. He is currently working as a senior designer in the Studio di Microelettronica, Pavia. His research interests are about high speed equalization and clock-data recovery techniques.

Paolo Viola was born in Pavia, Italy, in 1974. He received the Laurea degree in electronics engineering from the University of Pavia, Italy, in 1999.

In 2001, he joined STMicroelectronics, Italy, where he was involved in the design of high speed ADCs. In 2003 he started working on high speed links. Since January 2006, he has been with the Studio di Microelettronica, Pavia, as a senior designer, working on the behavioral modelling and circuit design of high speed serial interfaces.

Matteo Pisati was born in Cremona, Italy, in 1976. He received the Laurea degree (summa cum laude) and the Ph.D. in electronics engineering from the University of Pavia, Italy, in 2001 and 2005, respectively, working on system analysis and design of high speed analog CMOS circuits for fiber optic and wireline applications. During this period, he spent six months at Conexant Systems, Newport Beach, CA, where he focused on the architectural analysis of clock and data recovery.

In 2005 he joined STMicroelectronics, where he is involved in the design of high speed analog and mixed signal circuits for Serial Interfaces applications. He is presently working in the Studio di Microelettronica, Pavia, as a design engineer in the Serial Interfaces group.

Emanuele Depaoli was born in Pavia, Italy, in 1980. He received the Laurea degree in electronics engineering from the University of Pavia, Italy, in 2004. His Laurea thesis focused on the study of a RF front-end for a multistandard concurrent receiver based on LNA with positive feedback.

In 2004–2005, he was involved in an Italian National Program aimed at the design of a multi-standard receiver for WLAN. In December 2005, he joined STMicroelectronics in the Studio di Microelettronica, Pavia, as an analog design engineer. Presently, he is working in the area of low-power, high-speed serial interfaces.
Davide Sanzogni was born in Breno, Italy, in 1979. He received the Laurea and the Ph.D. degree in electrical engineering from the University of Pavia, Pavia, Italy, in 2004 and 2007, respectively. During his Laurea thesis he studied high dynamic range mixers for mobile phone communication. His Ph.D. research was focused on high-speed CMOS circuits, with particular focus on continuous-time and discrete-time linear equalizers. In 2007, he joined STMicroelectronics inside the Studio di Microelettronica, Pavia, in the Serial Interface team. His main activities are in the field of high-speed serial data link CMOS interfaces.

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Dr. Svelto is member of the technical program committee of the International Solid State Circuits Conference and has been a member of Custom Integrated Circuits Conference, Bipolar/BiCMOS Circuits Technology Meeting and European Solid State Circuits Conference. He served as Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (2003–2007), and as Guest Editor for a special issue on the same journal in March 2003. He is co-recipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2003 Best Paper Award.